APPLICATION NOTE

AN178
Modeling the PLL

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Modeling the PLL AN178

INTRODUCTION

The phase-locked loop is a feedback system comprised of a phase comparator, a low-pass filter and an error amplifier in the forward signal path and a voltage-controlled oscillator (VCO) in the feedback path. The block diagram of a basic PLL system is shown in Figure 1. Perhaps the single most important point to realize when designing with the PLL is that it is a feedback system and, hence, is characterized mathematically by the same equations that apply to other, more conventional feedback systems. However, the parameters in the equations are somewhat different since the feedback error signal in the phase locked system is a phase rather than a current or voltage signal, as is usually the case in conventional feedback systems.

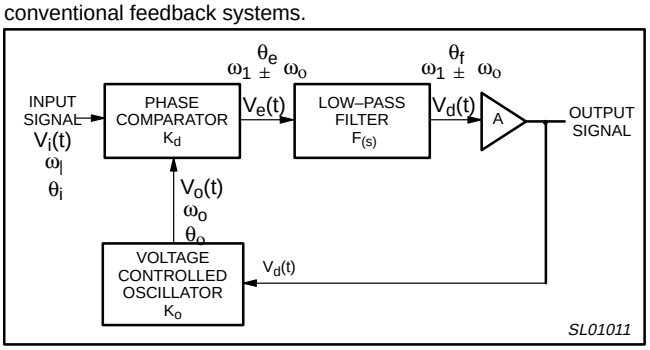


Figure 1. Block Diagram of Phase-Locked Loop

PHASE-LOCKED LOOP OPERATION

The basic principle of the PLL operation can be briefly explained as follows:

With no signal input applied to the system, the VCO control voltage $V_d(t)$ is equal to zero. The VCO operates at a set frequency, f_O' (or the equivalent radian frequency ω_O') which is known as the free-running frequency. When an input signal is applied to the system, the phase comparator compares the phase and the frequency of the input with the VCO frequency and generates an error voltage $V_e(t)$ that is related to the phase and the frequency diHerence between the two signals. This error voltage is then filtered, amplified, and applied to the control terminal of the VCO. In this manner, the control voltage $V_d(t)$ forces the VCO frequency to vary in a direction that reduces the frequency difference between ω_O and the input signal. If the input frequency ω_I is sufficiently close to ω_O, the feedback nature of the PLL causes the VCO to synchronize or lock with the incoming signal. Once in lock, the VCO frequency is identical to the input signal except for a finite phase difference.

This net phase difference of θ_e where

$$\theta_e = \theta_o - \theta_i \quad (1)$$

is necessary to generate the corrective error voltage V_d to shift the VCO frequency from its free-running value to the input signal frequency ω_I and thus keep the PLL in lock. This selfcorrecting ability of the system also allows the PLL to track the frequency changes of the input signal once it is locked. The range of frequencies over which the PLL can maintain lock with an input signal is defined as the “lock range” of the system. The band of frequencies over which the PLL can acquire lock with an incoming signal is known as the “capture range” of the system and is never greater than the lock range.

Another means of describing the operation of the PLL is to observe that the phase comparator is in actuality a multiplier circuit that mixes the input signal with the VCO signal. This mix produces the sum and difference frequencies $\omega_I \pm \omega_O$ shown in Figure 1. When the loop is in lock, the VCO duplicates the input frequency so that the difference frequency component ($(\omega_I \times \omega_O)$) is zero; hence, the output of the phase comparator contains only a DC component. The low-pass filter removes the sum frequency component ($\omega_I + \omega_O$) but passes the DC component which is then amplified and fed back to the VCO. Notice that when the loop is in lock, the difference frequency component is always DC, so the lock range is independent of the band edge of the low-pass filter.

LOCK AND CAPTURE

Consider now the case where the loop is not yet in lock. The phase comparator again mixes the input and VCO signals to produce sum and difference frequency components. However, the difference component may fall outside the band edge of the low-pass filter and be removed along with the sum frequency component. If this is the case, no information is transmitted around the loop and the VCO remains at its initial free-running frequency. As the input frequency approaches that of the VCO, the frequency of the difference component decreases and approaches the band edge of the low-pass filter. Now some of the difference component is passed, which tends to drive the VCO towards the frequency of the input signal. This, in turn, decreases the frequency of the difference component and allows more information to be transmitted through the low-pass filter to the VCO. This is essentially a positive feedback mechanism which causes the VCO to snap into lock with the input signal. With this mechanism in mind, the term “capture range” can again be defined as ‘the frequency range centered about the VCO initial free-running frequency over which the loop can acquire lock with the input signal’. The capture range is a measure of how close the input signal must be in frequency to that of the VCO to acquire lock. The “capture range” can assume any value within the lock range and depends primarily upon the band edge of the low-pass filter together with the closed-loop gain of the system. It is this signal capturing phenomenon which gives the loop its frequency-selective properties.

It is important to distinguish the “capture range” from the “lock range” which can, again, be defined as ‘the frequency range usually centered about the VCO initial free–running frequency over which the loop can track the input signal once lock has been achieved’.

When the loop is in lock, the difference frequency component at the output of the phase comparator (error voltage) is DC and will always be passed by the low-pass filter. Thus, the lock range is limited by the range of error voltage that can be generated and the corresponding VCO frequency deviation produced. The lock range is essentially a DC parameter and is not affected by the band edge of the low-pass filter.

THE CAPTURE TRANSIENT

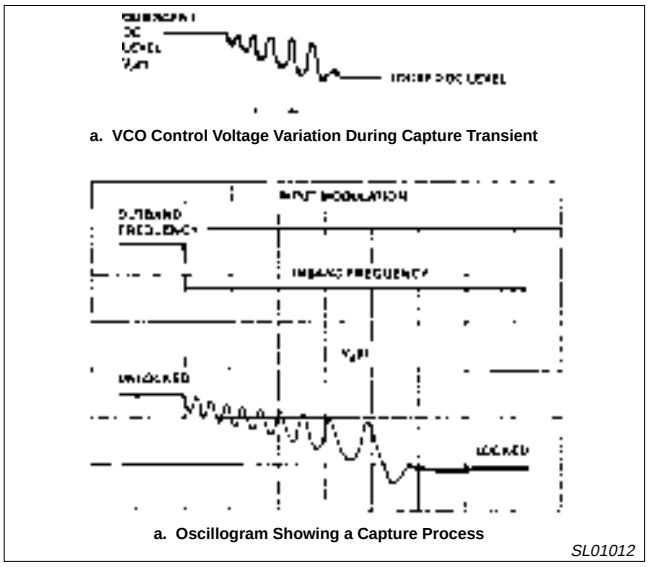
The capture process is highly complex and does not lend itself to simple mathematical analysis. However, a qualitative description of the capture mechanism may be given as follows. Since frequency is the time derivative of phase, the frequency and the phase errors in the loop can be related as

$$\Delta\omega = \frac{d\theta_e}{d_t} \quad (2)$$

where $\Delta\omega$ is the instantaneous frequency separation between the signal and VCO frequencies and θ_e is the phase difference between the input signal and VCO signals.

If the feedback loop of the PLL were opened between the low-pass filter and the VCO control input, then for a given condition of ω_O and ω_I the phase comparator output would be a sinusoidal beat note at a fixed frequency $\Delta\omega$. If ω_I and ω_O were sufficiently close in

frequency, this beat note would appear at the filter output with negligible anenuation.



a. VCO Control Voltage Variation During Capture Transient

a. Oscillogram Showing a Capture Process

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Figure 2. Asynchronous Error Beat Frequency During the Capture Transient

Now suppose that the feedback loop is closed by connecting the low-pass filter output to the VCO control terminal. The VCO frequency will be modulated by the beat note. When this happens, $\Delta\omega$ itself will become a function of time. If, during this modulation process, the VCO frequency moves closer to

$$\omega_I, \text{ (i.e., decreasing } \Delta\omega), \text{ then } \frac{d\theta_e}{dt} \text{ decreases}$$

and the output of the phase comparator becomes a slowly varying function of time. Similarly, if the VCO is modulated away from

$$\omega_I, \quad \frac{d\theta_e}{dt} \text{ increases and the error voltage}$$

becomes a rapidly varying function of time. Under this condition the beat note waveform no longer looks sinusoidal; it looks like a series of aperiodic cusps, depicted schematically in Figure 2a. Because of its asymmetry, the beat note waveform contains a finite DC component that pushes the average value of the VCO toward ω_I and lock is established. When the system is in lock, $\Delta\omega$ is equal to zero and only a steady-state DC error voltage remains.

Figure 2b displays an oscillogram of the loop error voltage $V_d(t)$ in an actual PLL system during the capture process. Note that as lock is approached, $\Delta\omega$ is reduced, the low-pass filter anenuation becomes less, and the amplitude of the beat note increases.

The total time taken by the PLL to establish lock is called the *pull-in time*. Pull-in time depends on the initial frequency and phase differences between the two signals as well as on the overall loop gain and the low-pass filter bandwidth. Under certain conditions, the pull-in time may be shorter than the period of the beat note and the loop can lock without an oscillatory error transient.

A specific case to illustrate this is shown in Figure 3. The 565 PLL is shown acquiring lock within the first cycle of the input signal. The PLL was able to capture in this short time because it was operated as a first-order loop (no low-pass filter) and the input tone-burst frequency was within its lock and capture range.

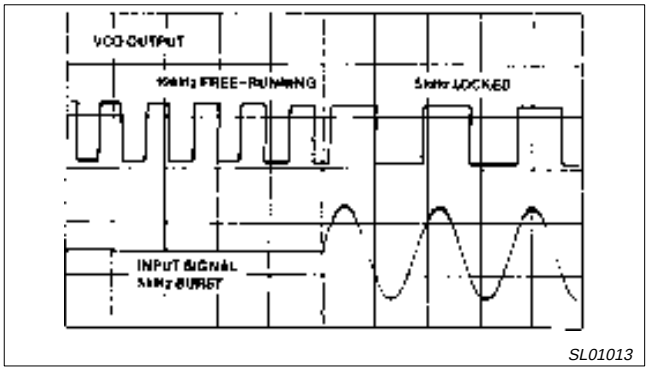

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Figure 3. Exhibited by First-Order Fast Capture Transient

EFFECT OF THE LOW-PASS FILTER

In the operation of the loop, the low-pass filter serves a dual function.

First, by anenuating the high frequency error components at the output of the phase comparator, it enhances the interference-rejection characteristics; second, it provides a short-term memory for the PLL and ensures a rapid recapture of the signal if the system is thrown out of lock due to a noise transient. Decreasing the low-pass filter bandwidth has the following effects on system performance (Long Time Constant):

a. The capture process becomes slower, and the pull-in time increases.

b. The capture range decreases.

c. Interference-rejection properties of the PLL improve since the error voltage caused by an interfering frequency is attenuated further by the low-pass filter.

d. The transient response of the loop (the response of the PLL to sudden changes of the input frequency within the capture range) becomes underdamped.

The last effect also produces a practical limitation on the low-pass loop filter bandwidth and roll-off characteristics from a stability standpoint. These points will be explained further in the following analysis.

MATHEMATICALLY DEFINING PLL OPERATION

As mentioned previously, the phase comparator is basically an analog multiplier that forms the product of an RF input signal, $V_i(t)$, and the output signal, $v_o(t)$, from the VCO. Refer to Figure 1 and assume that the two signals to be multiplied can be described by

$$V_i(t) = V_I \sin \omega_I t \tag{3}$$

$$V_o(t) = V_O \sin (\omega_O t \quad \theta_e) \tag{4}$$

where ω_I, ω_O, and θ_e are the frequency and phase difference (or phase error) characteristics of interest. The product of these two signals is an output voltage given by

$$V_e(t) = K_1 V_I V_O (\sin\omega_I t) [\sin(\omega_O t \quad \theta_e)] \tag{5}$$

where K_1 is an appropriate dimensional constant. Note that the amplitude of $v_e(t)$ is directly proportional to the amplitude of the input signal V_I. The two cases of an unlocked loop ($\omega_I \neq \omega_O$) and of a locked loop ($\omega_I = \omega_O$) are now considered separately.

Unlocked State ($\omega_I \neq \omega_O$)
When the two frequencies to the phase comparator are not synchronized, the loop is not locked. Furthermore, the phase angle difference θ_e in Equations 4 and 5 is meaningless lor this case since it can be eliminated by appropriately choosing the time origin.

Using trigonometric identities, Equation 5 can be rewritten as

$$v_e(t) = \frac{K_1 V_I V_O}{2} [\cos(\omega_I - \omega_O)t - \cos(\omega_I \quad \omega_O)t] \tag{6}$$

When $v_e(t)$ is passed through the low-pass filter, F(s), the sum frequency component is removed, leaving

$$v_f(t) = K_2 V_I V_O \cos(\omega_I - \omega_O)t \tag{7}$$

where K_2 is a constant. After amplification, the control voltage for the VCO appears as

$$v_d(t) = AK_2 V_I V_O \cos(\omega_I - \omega_O)t \tag{8}$$

This equation shows that a beat frequency effect is established between ω_I and ω_O, causing the VCO's frequency to deviate by $\pm\Delta\omega$ from ω_O' in proportion to the signal amplitude ($AK_2V_IV_O$) passing through the filter. If the amplitude of V_I is sufficiently large and if signal limiting or saturation does not occur, the VCO output frequency will be shifted from ω_O' by some $\Delta\omega$ until lock is established where

$$\omega_I = \omega_O = \omega_O \pm \Delta\omega \tag{9}$$

If lock cannot be established, then either V_I is too small to drive the VCO to produce the necessary $\pm\Delta\omega$ deviation or ω_I is beyond the dynamic range of the VCO, i.e., ω_I >< ω_O' $\pm\Delta\omega$. Remedies for these no lock conditions are:

1. Increase Vl either internally or externally to the loop by providing additional amplification.
2. Increase the internal loop gain by adjusting upward (larger -3dB frequency) the response of the low-pass filter.
3. Shift ω_O' closer to the expected ω_I. Establishing frequency lock leads to the second case where $\omega_I = \omega_O$.

Locked State ($\omega_I = \omega_O$)
When ω_I and ω_O are frequency synchronized, the output signal from the phase comparator for $\omega_I = \omega_O = \omega$ and a phase shift of θ_e is

$$v_e(t) = K_1 V_I V_O(\sin\omega t) \sin(\omega t \quad \theta_e) \tag{10}$$

$$= \frac{K_1 V_I V_O}{2}[\cos\theta_e - \cos(2\omega t \quad \theta_e)]$$

The low-pass filter removes the high frequency, AC component of $v_e(t)$, leaving only the DC component. Thus,

$$v_f(t) = K_2 V_I V_O \cos\theta_e \tag{11}$$

After amplification the DC voltage driving the VCO and maintaining lock within the loop is

$$v_d(t) = V_D = AK_2 V_I V_O \cos\theta_e \tag{12}$$

Suppose ω_I and ω_O are perfectly synchronized to the free-running frequency ω_O'. For this case, V_D will be zero, indicating that θ_e must be $\pm 90°$. Thus V_D is proportional to the phase difference or phase error between θ_i and θ_o centered about a reference phase angle of $\pm 90°$. If ω_I changes slightly from ω_O', the first effect will be a change in θ_e from $\pm 90°$. V_D will adjust and settle out to some non-zero value to correct ω_O; under this condition frequency lock is maintained with $\omega_I = \omega_O$. The phase error will be shifted by some amount $\Delta\theta$ from the reference phase angle of $\pm 90°$. This concept can be simplified by redefining θ_e as

$$\theta_e = \theta_r \pm \Delta\theta \tag{13}$$

where θ_r, is the inherent, reference phase shift of $\pm 90°$ and $\Delta\theta$ is the departure from this reference value. Now the VCO control voltage becomes

$$v_D = AK_1 V_I V_O \cos(\theta_r \pm \Delta\theta) = \pm AK_2 v_I V_O \sin\Delta\theta \tag{14}$$

Since the sine function is odd, a momentary change in $\Delta\theta$ contains information about which way to adjust the VCO frequency to correct and maintain the locked condition. The maximum range over which $\Delta\theta$ changes can be tracked is -90° to +90°. This corresponds to a θ_e range from 0 to 180°.

In addition to being an error signal, V_D represents the demodulated output of an FM input applied as $v_{in}(t)$ assuming a linear VCO characteristic. Thus, FM demodulation can be accomplished with the PLL without the inductively-tuned circuits that are employed with conventional detectors.

DETERMINING PLL MODEL PARAMETERS

Since the PLL is basically an electronic servo loop, many of the analytical techniques developed for control systems are applicable to phase-locked systems. Whenever phase lock is established between $v_i(t)$ and $v_o(t)$ the linear model of Figure 4 can be used to predict the performance of the PLL system. Here θ_i and θ_o represent the phase angles associated with the input/output waveshapes, respectively; F(s) represents a generalized voltage transfer function for the low-pass filter in the s complex frequency domain; and K_d and K_o are conversion gains of the phase comparator and VCO, respectively, each having units as shown. The 1/s term associated with the VCO accounts for the inherent 90° phase shift in the loop since the VCO converts a voltage to a frequency and since phase is the integral of frequency. Thus the VCO functions as an integrator in the feedback loop.

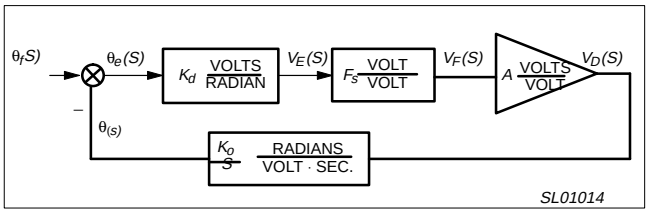


Figure 4. Linear Model of PLL System

Specific values of K_d and K_o for all of Philips Semiconductors general purpose PLLs can be found in the sections describing the particular loop of interest. However, sometimes it may be desired to determine these conversion gains exactly for a specific device. The measurement scheme shown in Figure 5 can be used to determine K_d and Ko for a loop under lock. The function of the Khron-Hite filters is to extract the fundamental sinusoidal frequency component of their square wave inputs for application to the Gain-Phase Meter. If the input signal from the Function Generator is sinusoidal, then the first Khron-Hite filter may be eliminated. It is recommended to use high impedance oscilloscope probes so as to not distort the input of VCO waveshapes, thereby potentially altering their phase relationships. The frequency counter can be driven from the scope as shown, or connected directly to the input or VCO, provided its input impedance is large.

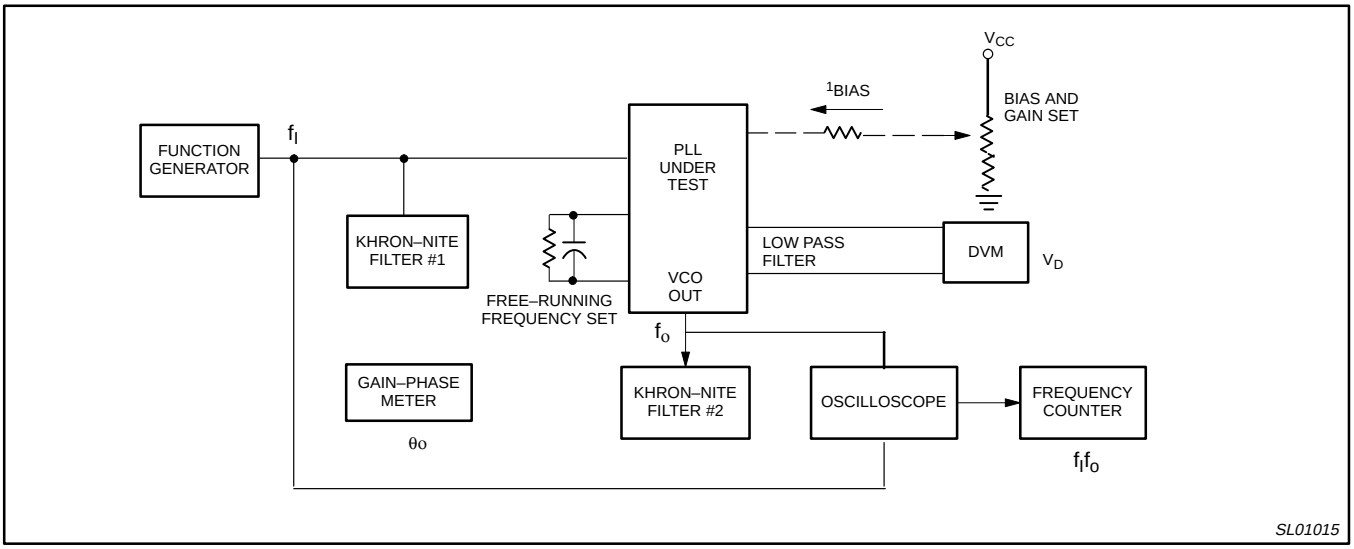


Figure 5. Measurement Scheme for K_d and K_o Determinations

The procedure to follow for obtaining K_d and K_o is as follows:

1. Establish the desired external bias and gain conditions for the PLL under test.
2. With the Function Generator turned off, set the free-running frequency of the loop via the timing capacitor and timing resistor if appropriate. Monitor f_O' with the Frequency Counter.
3. Turn on the Function Generator and check to make sure the amplitude of the input signal is appropriate for the particular loop under test.
4. Adjust the input frequency for lock. Lock is discernable on a dual-trace scope when the input and VCO waveforms are synchronized and stationary with respect to each other. One should be especially careful to check that locking has not occurred between the VCO and some harmonic frequency. Carefully inspect both waveshapes, making sure each has the same period. (If a second Frequency Counter is available, an alternate scheme can be used to confirm frequency locking. One frequency counter is used to monitor the input signal frequency, and the second counter is used for the VCO frequency. When the two counters display the same frequency, the PLL is locked.)
5. Set the input frequency to the free-running frequency and note the Gain-Phase Meter display. It should be approximately 90° ±10° nominally. Record the phase error, θ_e, the VCO control voltage, V_D, and the input frequency, f_I.
6. Adjust f_I for frequencies above and below f_O' and record θ_e and V_D for each f_I, as appropriate.
7. Making a plot of V_D versus θ_e is useful for checking the measurement data and the system's linearity. The slope of this plot ($\Delta V_D/\Delta\theta_e$) is K_d in units of V/°. Multiplying this slope by $180/\pi$ gives the desired K_d in volts/radian.
8. A plot of $f_I = f_O$ versus V_D while the loop remains locked will check the VCO linearity. The slope of this plot is K_o at the particular free-running frequency. The units of slope taken directly from the graph are Hz/V. Multiplying this slope figure by 2π gives the desired K_o in units of radians/ volt-sec.

K_d is generally constant over wide frequency ranges, but is linearily related to the input signal amplitude. K_o is constant with input signal level but does vary linearily with f_O'. Often it is convenient to specify a normalized K_o as

$$K_{O(norm)} = \frac{K_O \frac{rad}{V}}{f_O} \quad (15)$$

The K_o value at any desired free-running frequency then can be estimated as

$$K_O \text{ (@ any\% } f_O \text{)} = K_{o(norm)} f_O \quad (16)$$

AThe loop gain for the PLL system is

$$K_v = K_d K_o A \quad (17)$$

(Often when the gain A is due to an amplifier internal to the IC, A will be included in either K_d or K_o. This is further illustrated in the article on the 565 PLL.)

MODELING THE PLL SYSTEM WITH VARIOUS LOW-PASS FILTERS

The open-loop transfer function for the PLL is

$$T(s) = \frac{K_V F(s)}{s} \quad (18)$$

Using linear feedback analysis techniques, and assuming that the VCO is in the forward path, the closed-loop transfer characteristics H(s) can be related to the open-loop performance as

$$H(s) = \frac{T(s)}{1 \quad T(s)} \quad (19)$$

and the roots of the characteristic system polynomial can be readily determined by root-locus techniques.

From these equations, it is apparent that the transient performance and frequency response of the loop is heavily dependent upon the choice of filter and its corresponding transfer characteristic, F(s).

Zero-Order Filter — F(s) = 1

The simplest case is that of the first-order loop where F(s)= 1 (no filter). The closed-loop transfer function then becomes

$$H(s) = \frac{K_V}{S \quad K_V} \tag{20}$$

This transfer function gives the root locus as a function of the total loop gain K_V and the corresponding frequency response shown in Figure 6a. The open-loop pole at the origin is due to the integrating action of the VCO. Note that the frequency response is actually the amplitude of the difference frequency component versus modulating frequency when the PLL is used to track a frequency-modulated input signal. Since there is no low-pass filter in this case, sum frequency components are also present at the phase comparator output and must be filtered outside of the loop if the difference frequency component (demodulated FM) is to be measured.

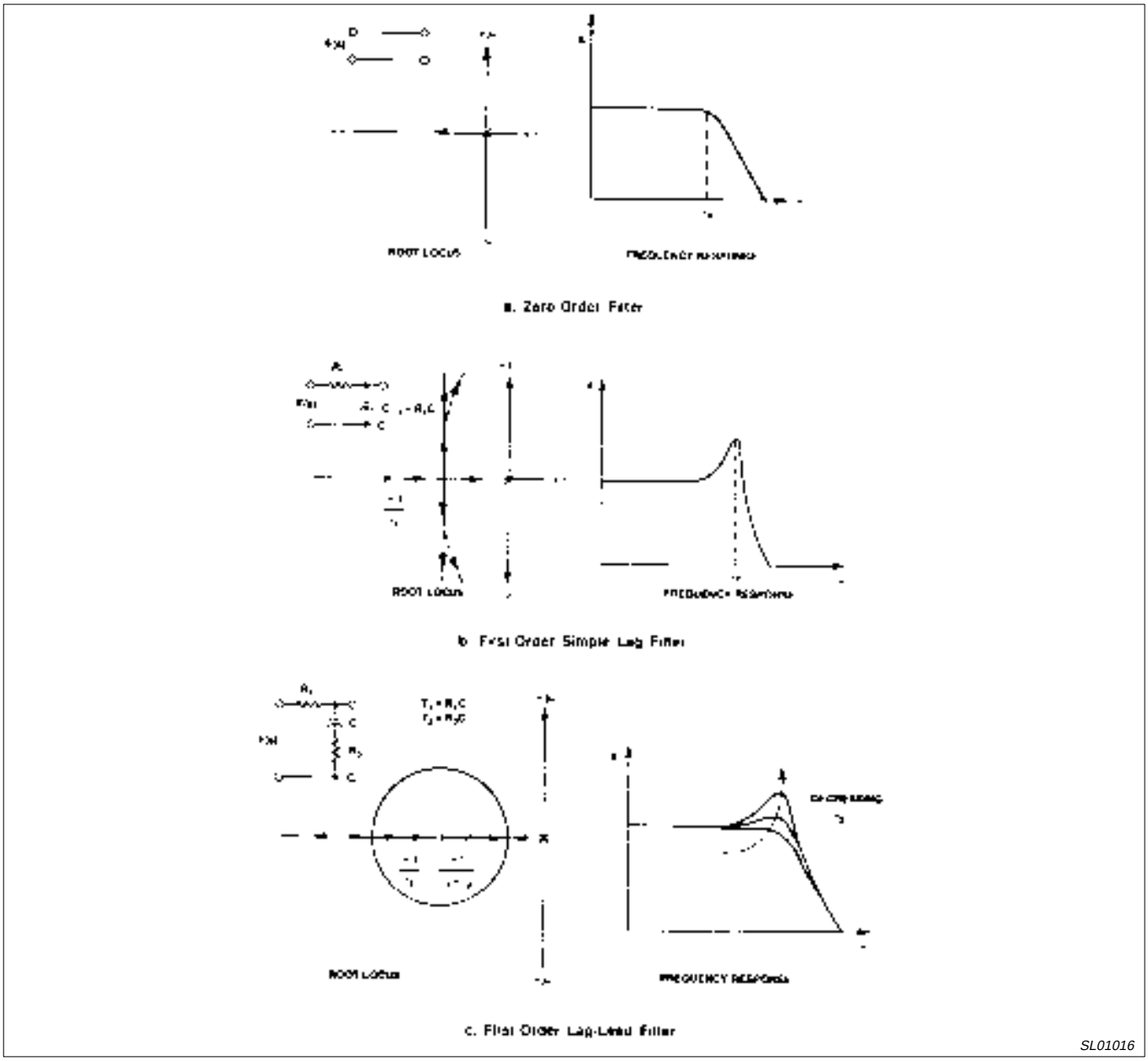


Figure 6. Root Locus and Frequency Response Plots

First-Order Filter

With the addition of a single-pole low-pass filter F(s) of the form

$$F(s) = \frac{1}{1 \quad {}_1 s} \tag{21}$$

where $\tau 1 = R_1 C_1$, the PLL becomes a second-order system with the root locus shown in Figure 6b. Again, an open-loop pole is located at the origin because of the integrating action of the VCO. Another open-loop pole is positioned on the real axis at $-1/\tau_1$ where τ_1 is the time constant of the low-pass filter.

One can make the following observations from the root locus characteristics of Figure 6b:

a. As the loop gain K_v increases for a given choice of τ_1, the imaginary part of the closed-loop poles increases: thus, the natural frequency of the loop increases and the loop becomes more and more under-damped.

b. If the filter time constant is increased, the real part of the closed-loop poles becomes smaller and the loop damping is reduced.

As in any practical feedback system, excess shifts or non-dominant poles associated with the blocks within the PLL can cause the root loci to bend toward the right half plane as shown by the dashed line in Figure 6b. This is likely to happen if either the loop gain or the filter time constant is too large and may cause the loop to break into sustained oscillations.

First-Order Lag-Lead Filter

The stability problem can be eliminated by using a lag-lead type of filter, as indicated in Figure 6c. This type of a filter has the transfer lock range. For the simple first-order lag filter function

$$F(s) = \frac{1 \quad {}_2 s}{1 \quad (\text{tau}_1 \quad {}_2) s} \tag{22}$$

where $\tau_2 = R_2 C$ and $\tau_1 = R_1 C$. By proper choice of R_2, this type of filter confines the root locus to the left half-plane and ensures stability. The lag-lead filter gives a frequency response dependent on the damping, which can now be controlled by the proper adjustment of τ_1 and τ_2. In practice, this type of filter is important because it allows the loop to be used with a response between that of the firstand second-order loops and it provides an additional control over the loop transient response. If $R_2 = 0$, the loop behaves as a second-order loop and as $R_2 \rightarrow \infty$, the loop behaves as a first-order loop due to a pole-zero cancellation. However, as first-order operation is approached, the noise bandwidth increases and interference rejection decreases since the high frequency error components in the loop are now attenuated to a lesser degree.

Second- and Higher-Order Filters

Second- and higher-order filters, as well as active filters, occasionally are designed and incorporated within the PLL to achieve a particular response not possible or easily obtained with zero or first-order filters. Adding more poles and more gain to the closedloop transfer function reduces the inherent stability of the loop. Thus the designer must exercise extreme care and utilize complex stability analysis if second-order (and higher) filters or active filters are to be considered.

CALCULATING LOCK AND CAPTURE RANGES

In terms of the basic gain expression in the and system, the lock range of the PLL ω_L can be shown to be numerically equal to the DC loop gain (2-sided lock range).

$$2\omega_L \quad 4 \; f_L \quad K_V F(0) \tag{23}$$

where F(O) is the value of the low-pass filters transfer function at DC.

Since the capture range ω_C denotes a transient condition, it is not as readily derived as the lock range. However, an approximate expression for the capture range can be wrinen as (2-sided capture range).

$$2\omega_C = 4 \; f_C \quad K_V \mid F(i\omega_C) \mid \tag{24}$$

where $F(i\omega_C)$ is the magnitude of the low-pass filter transfer function evaluated at ω_C. Solution of Equation 24 frequently involves a “trial and error” process since the capture range is a function of itself. Note that at all times the capture range is smaller than the lock rage. For the simple first-order lag filter of Figure 6b, the capture range can be approximated as

$$2\omega_c \quad 2 \quad \frac{\overline{\omega_L}}{1} = 2 \quad \frac{\overline{K_V}}{1} \tag{25}$$

This approximation is valid for

$$1 \quad \frac{1}{2\omega_L} \tag{26}$$

Equations 23 and 24 show that the capture range increases as the low-pass filter time constant is decreased, whereas the lock range is unaffected by the filter and is determined solely by the loop gain.

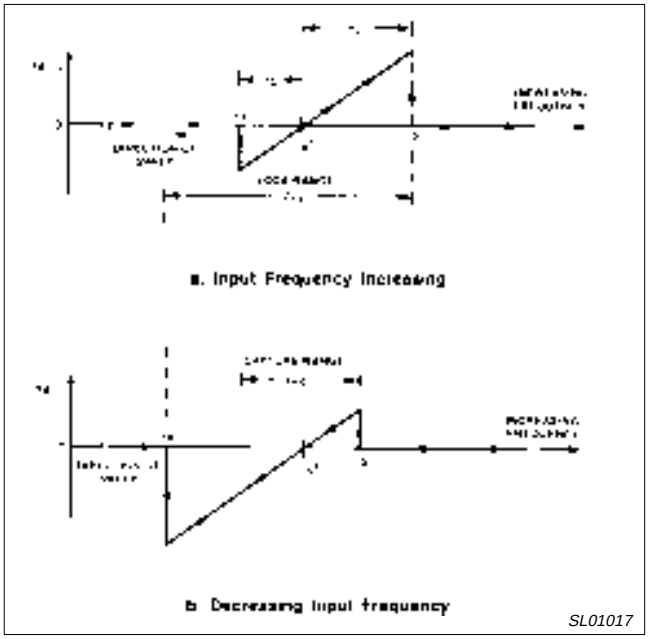


Figure 7. Typical PLL Frequency-to-Voltage Transfer Characteristics

Figure 7 shows the typical frequency-to-voltage transfer characteristics of the PLL. The input is assumed to be a sine wave whose frequency is swept slowly over a broad frequency range. The vertical scale is the corresponding loop error voltage. In Figure 7a, the input frequency is being gradually increased. The loop does not respond to the signal until it reaches a frequency ω_1, corresponding to the lower edge of the capture range. Then, the loop suddenly locks on the input and causes a negative jump of the loop error voltage. Next, V_d varies with frequency with a slope equal to the reciprocal of VCO conversion gain (1/Ko) and goes through zero as $\omega_I = \omega_O$'. The loop tracks the input until the input frequency reaches ω_2, corresponding to the upper edge of the lock range. The PLL then loses lock and the error voltage drops to zero. If the input frequency is swept slowly back, the cycle repeats itself, but is inverted, as shown in Figure 7b. The loop recaptures the signal at ω_3 and tracks it down to ω_4. The total capture and lock ranges of the system are:

$$2\omega_C = \omega_3 - \omega_1 \quad (27)$$

and

$$2\omega_L = \omega_2 - \omega_4 \quad (28)$$

Note that, as indicated by the transfer characteristics of Figure 7, the PLL system has an inherent selectivity about the free-running frequency, ω_O'. It will respond only to the input signal frequencies that are separated from ω_O' by less than ω_C or ω_L, depending on whether the loop starts with or without an initial lock condition. The linearity of the frequency-to-voltage conversion characteristics for the PLL is determined solely by the VCO conversion gain. Therefore, in most PLL applications, the VCO is required to have a highly linear voltage-to-frequency transfer characteristic.

DETERMINING LOOP RESPONSE

The transient response of a PLL can be calculated using the model of Figure 4 and Equations 18 and 19 as starting points. Combining these equations gives

$$H(s) = \frac{\theta_o(s)}{\theta_i(s)} = \frac{K_V F(s)}{s \quad K_V F(s)} \quad (29)$$

The phase error which keeps the system in lock is

$$\theta_e(s) = \theta_i(s) - \theta_o(s) \quad (30)$$

Define a phase error transfer function

$$E(s) \quad \frac{\theta_e(s)}{\theta_i(s)} = 1 - \frac{\theta_o(s)}{\theta_i(s)} = 1 - H(s) \quad (31)$$

As an example of the utilization of these equations, consider the most common case of a loop employing a simple first-order lag filter where

$$F(s) = \frac{1}{1 \quad s_{\ 1}} \quad (32)$$

For this filter, Equations 29 and 31 become

$$H(s) = \frac{K_{V\ 1}}{s \quad s_{\ 1} \quad K_{V\ 1}} \quad (33)$$

$$E(s) = \frac{s(s \quad 1_{\ 1})}{S \quad s_{\ 1} \quad K_{V\ 1}} \quad (34)$$

Both equations are second-order and have the same denominator which can be expressed as

$$D(s) = s^2 \quad s_{\ 1} \quad K_{V\ 1} = s^2 \quad 2\ \omega_n s \quad \omega_n^2 \quad (35)$$

Where ω_n and ζ are, respectively, the system's undamped natural frequency and damping factor defined as

$$\omega_n = \overline{K_{V\ 1}} \quad (36)$$

$$= \frac{1}{K_{V\ 1}} = \frac{\omega_n}{2K_V} \quad (37)$$

The system is considered overdamped for $\zeta > 1.0$, and critically damped $\zeta = 1.0$. Now examine this PLL system's response to various types of inputs.

Step-of-Phase Input

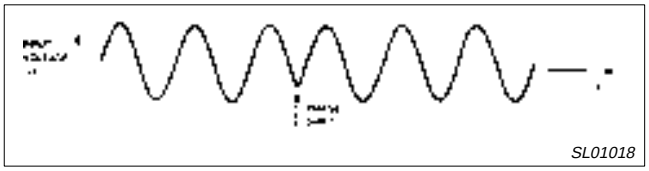


Figure 8. Input Signal Representing a Unit Step of Phase at Constant Frequency

Consider a unit step-of-phase as the input signal. This input is shown in Figure 8 and can be thought of as simply shifting the time axis by a unit step (one radian or one degree, depending upon the working units) while maintaining the same input frequency. Mathematically this input has the form

$$\theta_i(s) = \frac{1}{s} \quad (38)$$

The phase of VCO output and the system's phase error are represented by

$$\theta_o(s) = \frac{H(s)}{s} = \frac{\omega_n^2}{s(s^2 \quad 2\omega_{\ n}s \quad \omega_n^2} \quad (39)$$

$$\theta_o(s) = \frac{E(s)}{s} = \frac{s \quad 2\omega_{\ n}}{s^2 \quad 2\omega_{\ n}s \quad \omega_n^2} \quad (40)$$

(depending upon the working units) while maintaining the same input frequency. Mathematically this input has the form

$$\theta_o(t) = 1 \quad \frac{e - \omega_n t}{\overline{1 - \ ^2}} \sin(\omega_n t \quad \overline{1 - \ ^2} \quad (41)$$

$$\text{where} \quad = \arctan\frac{\overline{1 - \ ^2}}{} \quad (42)$$

and $\zeta \neq 1$.

$$\theta_e(t) = \frac{e - \omega_n(t)}{1 - \ ^2} \sin(\omega_n t \quad \overline{1 - \ ^2} \quad (43)$$

When $\zeta = 1$, these phase responses are

$$\theta_o(t) = 1 - (1 - \omega_n t)e - \omega_n t \quad (44)$$

and

$$\theta_e(t) = (1 \quad \omega_n t)e - \omega_n t \quad (45)$$

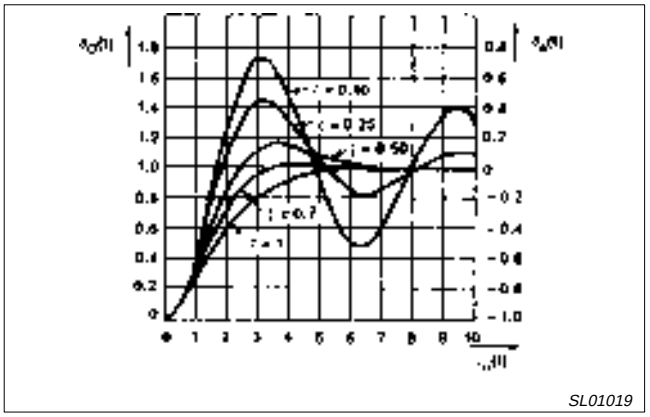


Figure 9. VCO Phase and Loop Phase Error Transient Responses for Various Damping Factors

Figure 9 is a plot of the VCO phase response and the phase error transient for various damping factors. Note from this figure that an underdamped system has overshoot which can cause the loop to break lock if this overshoot is too large. The critical condition for maintaining lock is to keep the phase error within the dynamic range for the phase comparator of -π/2 to π2 radians. For the underdamped case, the peak phase-error overshoot is

$$\theta_e(\max) = e^{-} \qquad \overline{1 - \quad ^2} \tag{46}$$

which must be less than π/2 to maintain lock. Lock can also be broken for the overdamped and critically-damped loops if the input phase shift is too large where the phase error exceeds ±π/2 radians.

The analysis and equations given are based upon the small-signal model of Figure 4. If the signal amplitudes become too large, one or more functional blocks in the system can saturate, causing a slew rate type limiting action that may break lock.

The *transient change* in the VCO frequency due to the unit step-of-phase input can be found by taking the time derivative of Equation 41 or alternatively by finding the inverse Laplace transform of

$$\omega_o(s) = s\theta_o(s) = \frac{\omega_n^2}{s^2 \quad 2\ \omega_n s \quad \omega_n^2} \tag{47}$$

which is

$$\omega_O(t) = \frac{\omega_n e^{-} \quad \omega_n t}{\overline{1 - \quad ^2}} \sin \omega_n t \quad \overline{1 - \quad ^2} \tag{48}$$

Unit Step-of-Frequency Input

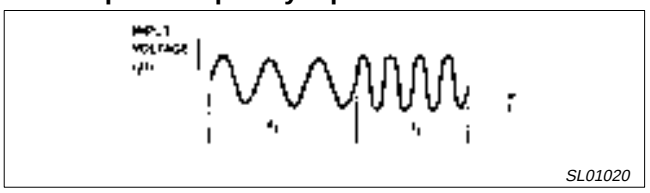


Figure 10. Input Signal for a Unit Step-of-Frequency at Constant Phase

This type of input occurs when the input frequency is instantaneously changed from one frequency to another as is done in FSK and modem applications. For this input, as shown in Figure 10,

$$\theta_i(s) = \frac{1}{s^2} \tag{49}$$

The VCO output phase is

$$\theta_o(s) = \frac{\omega_n^2}{s^2(s^2 \quad 2\ \omega_n s \quad \omega_n^2)} \tag{50}$$

The time expression for the VCO *phase change* is

$$\theta_o(t) = t - \frac{2}{\omega_n} \quad \frac{e^{-} \quad \omega_n t}{\omega_n \overline{1 - \quad ^2}} \sin(\omega_n t \quad \overline{1 - \quad ^2} \quad 2 \tag{51}$$

for $\zeta \neq 1$.

The time expression for the VCO *frequency change* for a unit step-of-frequency input is the same as the time response VCO phase change due to a step-of-phase input (Equation 41), or

$\omega_O(t)$ for frequency step input = $\theta_o(t)$ for phase step input. Thus

$$\omega_o(t) = 1 \quad \frac{e^{-} \quad \omega_n t}{\overline{1 - \quad ^2}} \sin(\omega_n t \quad \overline{1 - \quad ^2} \tag{52}$$

for $\zeta \neq 1$.

Unit Ramp-of-Frequency Input

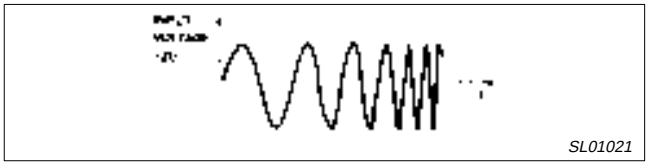


Figure 11. Input Signal for a Unit Ramp-of-Frequency Input

This form of input signal represents sweeping the input frequency at a constant rate and direction as shown in Figure 11. The amplitude and phase of the input remain constant; the input frequency changes linearly with time. Since the input signal to the PLL model is a phase, a unit ramp-of-frequency appears as a phase acceleration type input that can be mathematically described as

$$\theta_i(s) = \frac{1}{s^3} \tag{53}$$

The VCO output phase change is

$$\theta_o(s) = \frac{\omega_n^2}{s^3(s^2 \quad 2\ \omega_n s \quad \omega_n^2} \tag{54}$$

The time expression for the VCO phase change is

$$\theta_o(s) = \frac{t^2}{2} - \frac{2\ t}{\omega_n} \quad \frac{2}{\omega_n^2} [2\ (1 - \omega_n^2) \tag{55}$$

$$\frac{1 - 4\ ^2\omega_n^2 \quad 4\ ^2\omega_n^4}{1 - \quad ^2}^{\frac{1}{2}}$$

$$x\ e^{-\omega_n t} \sin(\omega_n t \quad \overline{1 - \quad ^2}$$

where $= \arctan \dfrac{\overline{1 - \quad ^2}}{(1 - 2\omega_n^2}$

and y is given in Equation 42.

PLL BUILDING BLOCKS VCO

Since three different forms of VCO have been used in the Philips Semiconductors PLL series, the VCO details will not be discussed until the individual loops are described. However, a few general comments about VCOs are in order.

When the PLL is locked to a signal, the VCO voltage is a function of the frequency of the input signal. Since the VCO control voltage is the demodulated output during FM demodulation, it is important that the VCO voltage-to-frequency characteristic be linear so that the output is not distorted. Over the linear range of the VCO, the conversin gain is given by K_O (in radian/V-sec)

$$K_O = \frac{\Delta\omega_O}{\Delta V_d} \quad (56)$$

Since the loop output voltage is the VCO voltage, we can get the loop output voltage as

$$\Delta V_d = \frac{\Delta\omega_O}{K_O} \quad (57)$$

The gain K_O can be found from the data sheet. When the VCO voltage is changed, the frequency change is virtually instantaneous.

Phase Comparator

All of Philips Semiconductors analog phase-locked loops use the same form of phase comparator — often called the doubly-balanced multiplier or mixer. Such a circuit is shown in Figure 12.

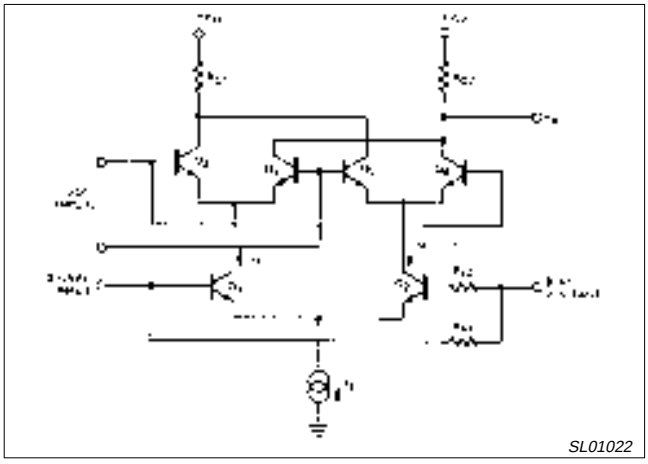


Figure 12. Integrated Phase Comparator Circuit

The input stage formed by transistors Q1 and Q2 may be viewed as a differential amplifier which has an equivalent collector resistance

R_C and whose differential gain at balance is the ratio of R_C to the dynamic emitter resistance, r_e, of Q1 and Q2.

$$A_d = \frac{R_C}{r_e} = \frac{R_C}{\frac{0.026}{I_E/2}} = \frac{R_C I_E}{0.052} \quad (58)$$

where I_E is the total DC bias current for the differential amplifier pair.

The switching stage formed by Q3 – Q6 is switched on and off by the VCO square wave. Since the collector current swing of Q2 is the negative of the collector current swing of Q1, the switching action has the effect of multiplying the differential stage output first by +1 and then by –1. That is, when the base of Q4 is positive, R_{C2} receives I_1 and when the base of Q6 is positive, R_{C2} receives $i_2 = i_1$.

Since the circuit is called a multiplier, performing the multiplication will gain further insight into the action of the phase comparator.

Consider an input signal which consists of two added components: a component at frequency ω_I which is close to the free-running frequency and a component at frequency ω_K which may be at any frequency. The input signal is

$$v_i(t) \quad v_k(t) = V_I \sin(\omega_i t \quad \theta_i) \quad v_k \sin(\omega_k t \quad \omega_k) \quad (59)$$

where θ_i and θ_k are the phase in relation to the VCO signal. The unity square wave developed in the multiplier by the VCO signal is

$$v_o(t) = \sum_{n=0} \frac{4}{(2n \quad 1)} \sin[(2n \quad 1)\omega_o t] \quad (60)$$

where ω_O is the VCO frequency. Multiplying the two terms, using the appropriate trigonometric relationships, and inserting the differential stage gain A_d gives:

$$v_e(t) = 2A_d \quad (61)$$

$$\left[\sum_{n=0} \frac{V_I}{(2n \quad 1)} \cos[(2n \quad 1)\ \omega_O t - \omega_I t - \theta_i] \right.$$

$$- \sum_{n=0} \frac{V_I}{(2n \quad 1)} \cos[(2n \quad 1)\ \omega_O t \quad \omega_I t \quad \theta_i]$$

$$\sum_{n=0} \frac{V_k}{(2n \quad 1)} \cos[(2n \quad 1)\ \omega_O t - \omega_I t - \theta_i]$$

$$\left. - \sum_{n=0} \frac{V_k}{(2n \quad 1)} \cos[(2n \quad 1)\ \omega_O t \quad \omega_I t \quad \theta_i] \right]$$

Assuming that temporarily V_k is zero, if ω_I is close to ω_O, the first term (n = 0) has a low frequency difference frequency component. This is the beat frequency component that feeds around the loop and causes lock-up by modulating the VCO. As ω_O is driven closer to ω_I, this difference component becomes lower and lower in frequency until $\omega_O = \omega_I$ and lock is achieved. The first term then becomes

$$V_e(t) = V_E = \frac{2A_d V_I}{(2n \quad 1)} \cos\theta_i \quad (62)$$

which is the usual phase comparator formula showing the DC component of the phase comparator during lock. This component must equal the voltage necessary to keep the VCO at ω_O. It is possible for ω_O to equal ω_I momentarily during the lock-up process and, yet, for the phase to be incorrect so that ω_O passes through ω_I without lock being achieved. This explains why lock is usually not achieved instantaneously, even when $\omega_I = \omega_O$ at t=0.

If $n \neq 0$ in the first term, the loop can lock when $\omega_I = (2n + 1)\omega_O$, giving the DC phase comparator component

$$V_e(t) = V_E = \frac{2A_d V_I}{(2n \quad 1)} \cos\theta_i \quad (63)$$

showing that the loop can lock to odd harmonics of the free-running frequency. The (2n + 1) term in the denominator shows that the phase comparator's output is lower for harmonic lock, which explains why the lock range decreases as higher and higher odd harmonics are used to achieve lock.

Note also that the phase comparator's output during lock is (assuming A_d is constant) also a function of the input amplitude V_I.

Thus, for a given DC phase comparator output V_E, an input amplitude decrease must be accompanied by a phase change. Since the loop can remain locked only for θ_i between 0 and 180°, the lower V_I becomes, the more the lock range is reduced.

Note from the second term that during lock the lowest possible frequency is $\omega_O + \omega_I = 2\omega_I$. A sum frequency component is always present at the phase comparator output. This component is usually greatly attenuated by the low-pass filter capacitor connected to the phase comparator output. However, when rapid tracking is required (as with high-speed FM detection or FSK), the requirement for a relatively high frequency cutoff in the low-pass filter may leave this component unattenuated to the extent that it interferes with detection. At the very least, additional filtering may be required to remove this component. Components caused by $n \neq 0$ in the second term are both attenuated and of much higher frequency, so they may be neglected.

Suppose that other frequencies represented by V_k are present. What is their effect for $V_k \neq 0$?

The third term shows that V_k introduces another difference frequency component. Obviously, if ω_k is close to ω_I, it can interfere with the locking process since it may form a beat frequency of the same magnitude as the desired locking beat frequency. However, suppose lock has been achieved so that $\omega_O = \omega_I$. In order for lock to be maintained, the average phase comparator output must be constant. If $\omega_O = \omega_k$ is relatively low in frequency, the phase θ_i must change to compensate for this beat frequency. Broadly speaking, any signal in addition to the signal to which the loop is locked causes a phase variation. Usually this is negligible since ω_k is often far removed from ω_I. However, it has been stated that the phase θ_i can move only between 0 and 180°. Suppose the phase limit has been reached and V_k appears. Since it cannot be compensated for, it will drive the loop out of lock. This explains why extraneous signals can result in a decrease in the lock range. If V_k is assumed to be an instantaneous noise component, the same effect occurs. When the full swing of the loop is being utilized, noise will decrease the lock or tracking range. This effect can be reduced by decreasing the cutoff frequency of the lowpass filter so that the $\omega_O - \omega_k$ is attenuated to a greater extent, which illustrates that noise immunity and out-band frequency rejection is improved (at the expense of capture range since $\omega_O - \omega_I$ is likewise attenuated when the low-pass filter capacitor is large.

The third term can have a DC component when ω_k is an odd harmonic of the locked frequency so that $(2n + 1)(\omega_O - \omega_I)$ is zero and θ_k makes its appearance. This will have an effect on θ_1 which will change the θ_1 versus frequency ω_I. This is most noticeable when the waveform of the incoming signal is, for example, a square wave. The θ_k term will combine with the θ_1 term so that the phase is a linear function of input frequency. Other waveforms will give different phase versus frequency functions. When the input amplitude V_I is large and the loop gain is large, the phase will be close to 90° throughout the range of VCO swing, so this effect is often unnoticed.

The fourth term is of little consequence except that if ω_k approaches zero, the phase comparator output will have a component at the locked frequency ω_O at the output. For example, a DC offset at the input differential stage will appear as a square wave of fundamental ω_O at the phase comparator output. This is usually small and well attenuated by the low-pass filter. Since many out-band signals or noise components may be present, many V_k terms may be combining to influence locking and phase during lock. Fortunately, only those close to the locked frequency need be considered.

Quadrature-Phase Detector (QPD)

The quadrature-phase detector action is exactly the same except that its output is proportional to the sine of the phase angle. When the phase θ_i is 90°, the quadraturephase detector output is then at its maximum, which explains why it makes a useful lock or amplitude detector. The output of the quadrature-phase detector is given by

$$V_q = \frac{2A_q V_I}{} \sin\theta_i \quad (64)$$

where V_I is the constant or modulated AM signal and $\theta_i \approx 90°$ in most cases so that sine $\theta_i = 1$ and

$$V_q = \frac{2A_q V_I}{} \quad (65)$$

This is the demodulation principle of the autodyne receiver and the basis for the 567 tone decoder operation.

INITIAL PLL SETUP CHOICES

In a given application, maximum PLL effectiveness can be achieved if the designer understands the tradeoffs which can be made. Generally speaking, the designer is free to select the frequency, lock range, capture range, and input amplitude.

FREE-RUNNING FREOUENCY SELECTION

Setting the center or free-running frequency is accomplished by selecting one or two external components. The center frequency is usually set in the center of the expected input frequency range. Since the loop's ability to capture is a function of the difference between the incoming and free-running frequencies, the band edges of the capture range are always an equal distance (in Hz) from the center frequency. Typically, the lock range is also centered about the free-running frequency. Occasionally, the center frequency is chosen to be offset from the incoming frequency so that the tracking range is limited on one side. This permits rejection of an adjacent higher or lower frequency signal without paying the penalty for narrow-band operation (reduced tracking speed).

All of Philips Semiconductors loops use a phase comparator in which the input signal is multiplied by a unity square wave at the VCO frequency. The odd harmonics present in the square wave permit the loop to lock to input signals at these odd harmonics. Thus, the center frequency may be set to, say, 1/3 or 1/5 of the input signal. The tracking range, however, will be considerably reduced as the higher harmonics are utilized.

The foregoing phase comparator discussion would suggest that the PLL cannot lock to subharmonics because the phase comparator cannot produce a DC component if ω_I is less than ω_O.

The loop can lock to both odd harmonic and subharmonic signals in practice because such signals often contain harmonic components at ω_O. For example, a square wave of fundamental $\omega_O/3$ will have a substantial component at ω_O to which the loop can lock. Even a pure sine wave input signal can be used for harmonic locking if the PLL input stage is overdriven. (The resultant internal limiting generates harmonic frequencies.) Locking to even harmonics or subharmonics is the least satisfactory, since the input or VCO signal must contain second harmonic distortion. If locking to even harmonics is desired, the duty cycle of the input and VCO signals must be shifted away from the symmetrical to generate substantial, even harmonic, content.

In evaluating the loop for a potential application, it is best to actually compute the magnitude of the expected signal component nearest ω_O. This magnitude can be used to estimate the capture and lock ranges.

All of Philips Semiconductors loops are stabilized against center frequency drift due to power supply variations. Both the 565 and the 567 are temperature-compensated over the entire military temperature range (-55 to +125°C). To benefit from this inherent stability, however, the designer must provide equally stable (or better) external components. For maximum cost effectiveness in some non-critical applications, the designer may wish to trade some stability for lower cost external components.

GUIDELINES FOR LOCK RANGE CONTROL

Two things limit the lock range. First, any VCO can swing only so far; if the input signal frequency goes beyond this limit, lock will be lost. Second, the voltage developed by the phase comparator is proportional to the product of both the phase and the amplitude of the in-band component to which the loop is locked. If the signal amplitude decreases, the phase difference between the signal and the VCO must increase in order to maintain the same output voltage and, hence, the same frequency deviation. The 564 contains an internal limiter circuit between the signal input and one input to the phase comparator. This circuit limits the amplitude of large input signals such as those from TTL outputs to approximately 100mV before they are applied to the phase comparator. The limiter significantly improves the AM rejection of the PLL for input signal amplitudes greater than 100mV.

This happens so often with low input amplitudes that even the full ±90° phase range of the phase comparator cannot generate enough voltage to allow tracking wide deviations. When this occurs, the effective lock range is reduced. Weak input signals cause a reduction of tracking capability and greater phase errors. Conversely, a strong input signal will allow the use of the entire VCO swing capability and keeps the VCO phase (referred to the input signal) very close to 90° throughout the range. Note that the lock range does not depend on the low-pass filter. However, if a low-pass filter is in the loop, it will have the effect of limiting the maximum rate at which tracking can occur. Obviously, the LPF capacitor voltage cannot change instantly, so lock may be lost when large enough step changes occur. Between the constant frequency input and the step-change frequency input is some limiting frequency slew rate at which lock is just barely maintained. When tracking at this rate, the phase difference is at its limit of 0° or 180°. It can be seen that if the LPF cutoff frequency is low, the loop will be unable to track as fast as if the LPF cutoff frequency is higher. Thus, when maximum tracking rate is needed, the LPF should have a high cutoff frequency. However, a high cutoff frequency LPF will attenuate the sum frequencies to a lesser extent so that the output contains a significant and often bothersome signal at twice the input frequency. The phase comparator's output contains both sum and difference frequencies. During lock, the difference frequency is zero, but the sum frequency of twice the locked frequency is still present. This sum frequency component can then be filtered out with an external low-pass filter.

INPUT LEVEL AMPLITUDE SELECTION

Whenever amplitude limiting of the in-band signal occurs, whether in the loop input stages or prior to the input, the lock and capture ranges become independent of signal amplitude.

Better noise and out-band signal immunity is achieved when the input levels are below the limiting threshold, since the input stage is in its linear region and the creation of cross-modulation components is reduced. Higher input levels will allow somewhat faster operation due to greater phase comparator gain and will result in a lock range which becomes constant with amplitude as the phase comparator gain becomes constant. Also, high input levels will result in a linear phase versus frequency characteristic.

CAPTURE RANGE CONTROL

There are two main reasons for making the low-pass filter time constant large. First, a large time constant provides an increased memory effect in the loop so that it remains at or near the operating frequency during momentary fading or loss of signal. Second, the large time constant integrates the phase comparator's output so that increased immunity to noise and out-band signals is obtained.

Besides the lower tracking rates attendant to large loop filters, other penalties must be paid for the benefits gained. The capture range is reduced and the capture transient becomes longer. Reduction of capture range occurs because the loop must utilize the magnitude of the difference frequency component at the phase comparator to drive the VCO towards the input frequency.

If the LPF cutoff frequency is low, the difference component amplitude is reduced and the loop cannot swing as far. Thus, the capture range is reduced.

LOCK-UP TIME AND TRACKING SPEED CONTROL

In tracking applications, lock-up time is normally of little consequence, but occasions do arise when it is desirable to keep lock-up time short to minimize data loss when noise or extraneous signals drive the loop out of lock. Lock-up time is of great importance in tone decoder type applications. Tracking speed is important if the loop is used to demodulate an FM signal. Although the following discussion dwells largely on lock-up time, the same comments apply to tracking speeds.

No simple expression is available which adequately describes the acquisition or lock-up time. This may be appreciated when we review the following factors which influence lock-up time.

a. Input phase

b. Low-pass filter characteristic

c. Loop damping

d. Deviation of input frequency from center frequency

e. In-band input amplitude

f. Out-band signals and noise

g. Center frequency

Fortunately, it is usually sufficient to know how to improve the lock-up time and what must be sacrificed to get faster lock-up. Consider an operational loop or tone decoder where occasionally the lock-up transient is too long. What can be done to improve the situation — keeping in mind the factors that influence lock?

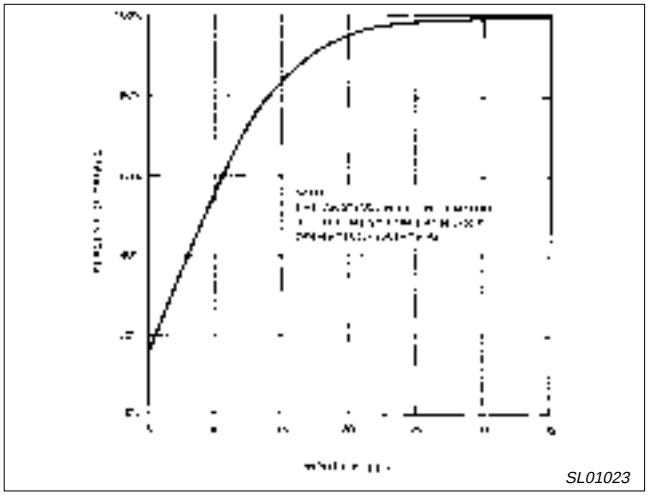


Figure 13. Probability of Lock vs Input Cycles

a. Initial phase relationship between incoming signal and VCO — This is the greatest single factor influencing the lock time. If the initial phase is wrong, it first drives the VCO frequency *away* from the input frequency so that the VCO frequency must walk back on the beat notes. Figure 13 gives a typical distribution of lock-up times with the input pulse initiated at random phase. The only way to overcome this variation is to send phase information all the time so that a favorable phase relationship is guaranteed at t = 0. For example, a number of PLLs or tone decoders may be weakly locked to low amplitude harmonics of a pulse train and the transmitted tone phase related to the same pulse train. Usually, however, the incoming phase cannot be controlled.

b. Low-pass filter — The larger the low-pass filter time constant, the longer will be the lock-up time. The lock-up time can be reduced by decreasing the filter time constant, but in doing so, some of the noise immunity and out-band signal rejection will be sacrificed. This is unfortunate, since this is what necessitated the use of a large filter in the first place. Also present will be a sum frequency (twice the VCO frequency) component at the low pass filter and greater phase jitter resulting from out-band signals and noise. In the case of the tone decoder (where control of the capture range is required since it specifies the device bandwidth) a lower value of low-pass capacitor automatically increases the bandwidth. Speed is gained only at the expense of added bandwidth.

c. Loop damping — A simple first-order lowpass filter of the form

$$F(s) = \frac{1}{1 \quad s} \tag{66}$$

produces a loop damping of

$$= 1\ 2\ \sqrt{\frac{1}{K_V}} \tag{67}$$

Damping can be increased not only by reducing π, as discussed above, but also by reducing the loop gain K_V. Using the loop gain reduction to control bandwidth or capture and lock ranges achieves better damping for narrow bandwidth operation. The penalty for this damping is that more phase comparator output is required for a given deviation so that phase errors are greater and noise immunity is reduced. Also, more input drive may be required for a given deviation.

d. Input frequency deviation from free-running frequency — Naturally, the further an applied input signal is from the free-running frequency of the loop, the longer it will take the loop to reach that frequency due to the charging time of the low-pass filter capacitor. Usually, however, the effect of this frequency deviation is small compared to the variation resulting from the initial phase uncertainty. Where loop damping is very low, however, it may be predominant.

e. In-band input amplitude — Since input amplitude is one factor in the phase comparator's gain K_d, and since K_d is a factor in the loop gain K_V damping is also a function of input amplitude. When the input amplitude is low, the lock-up time may be limited by the rate at which the low-pass capacitor can charge with the reduced phase comparator output (see d above).

f. Out-band signals and noise — Low levels of extraneous signals and noise have little effect on the lock-up time, neither improving or degrading it. However, large levels may overdrive the loop input stage so that limiting occurs, at which point the in-band signal starts to be suppressed. The lower effective input level can cause the lock-up time to increase, as discussed in e above.

g. Center frequency — Since lock-up time can be described in terms of the number of cycles to lock, fastest lock-up is achieved at higher frequencies. Thus, whenever a system can be operated at a higher frequency, lock will typically take place faster. Also, in systems where different frequencies are being detected, the higher frequencies, on the average, will be detected before the lower frequencies.

However, because of the wide variation due to initial phase, the reverse may be true for any single trial.

PLL MEASUREMENT TECHNIQUES

This section deals with measurements of PLL operation. The techniques suggested are meant to help the designer in evaluating the performance of the PLL during the initial setup period as well as to point out some pitfalls that may obscure loop evaluation. Recognizing that the test equipment may be limited, techniques are described which require a minimum of standard test items.

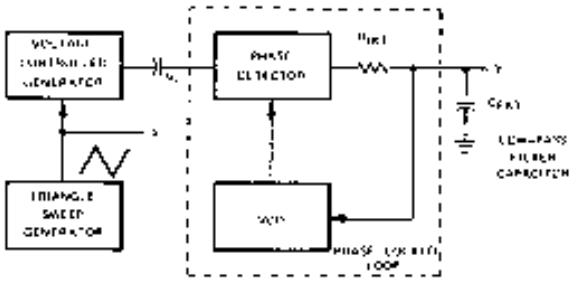
The majority of the PLL tests described can be done with a signal generator, a scope and a frequency counter. Most laboratories have these. A low cost digital voltmeter will facilitate accurate measurement of the VCO conversion gain. Where the need for a FM generator arises, it may be met in most cases by the VCO of a Philips Semiconductors PLL. Any of the loops may be set up to operate as a VCO by simply applying the modulating voltage to the low-pass filter terminal(s). The resulting generator may be checked for linearity by using the counter to check frequency as a function of modulating voltage. Since the VCOs may be modulated right down to DC, the calibration may be done in steps. Moreover, loop measurements may be made by applying a constant frequency to the loop input and the modulating signal to the low-pass filter terminal to simulate the effect of a FM input so that an FM generator may be omitted for many measurements.

FREE-RUNNING FREQUENCY

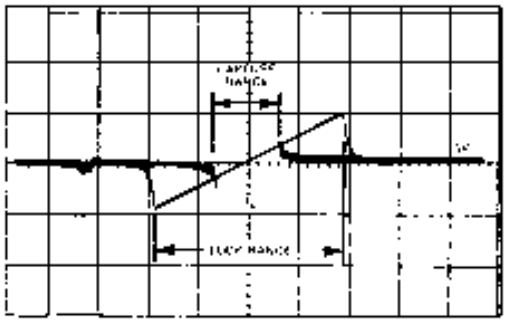
Free-running frequency measurements are easily made by connecting a frequency counter or oscilloscope to the VCO output of the loop. The loop should be connected in its final configuration with the chosen values of input, bypass, and low-pass filter capacitors. No input signal should be present. As the free-running frequency is read out, it can be adjusted to the desired value by the adjustment means selected for the particular loop. It is important not to make the frequency measurement directly at the timing capacitor, unless the capacity added by the measurement probe is much less than the timing capacitor value, since the probe capacity will then cause a frequency error.

When the frequency measurement is to be converted to a DC voltage for production readout or automated testing, a calibrated phase-locked loop can be used as a frequency meter.

CAPTURE AND LOCK RANGES



a. Measurement Setup



b. Oscilloscope Display

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Figure 14. Capture and Lock Ranges

Figure 14a shows a typical measurement setup for capture and lock range measurements. The signal input from a variable frequency oscillator is swept linearly through the frequency range of interest and the loop FM output is displayed on a scope or (at low frequencies) X-Y recorder. The sweep voltage is applied to the X axis.

Figure 14b shows the type of trace which results. The lock range is given by the outer lines on the trace, which are formed as the incoming frequency sweeps away from the center frequency. The inner trace, formed as the frequency sweeps toward the center frequency, designates the capture range. Linearity of the VCO is revealed by the straightness of the trace portion within the lock range. The slope ($\Delta f/\Delta V$) is the conversion gain K_o for the VCO at the particular free-running frequency.

By using the sweep technique, the effect on free-running frequency, capture range, and lock range of the input amplitude, supply voltage, low-pass filter and temperature can be examined.

Because of the lock-up time duration and variation, the sweep frequency must be much lower than the free-running frequency, especially when the capture range is below 10% of the free-running frequency. Otherwise, the apparent capture and lock range will be functions of sweep frequency. It is best to start sweeping as slowly as possible and, if desired, increase the rate until the capture range begins to show an apparent reduction — indicating that the sweep is too fast. Typical sweep frequencies are in the range of 1/1000 to 1/100,000 of the free-running frequency. In the case of the 567, the quadrature detector output may be similarly displayed on the Y axis, as shown in Figure 15, showing the output level versus frequency for one value of input amplitude.

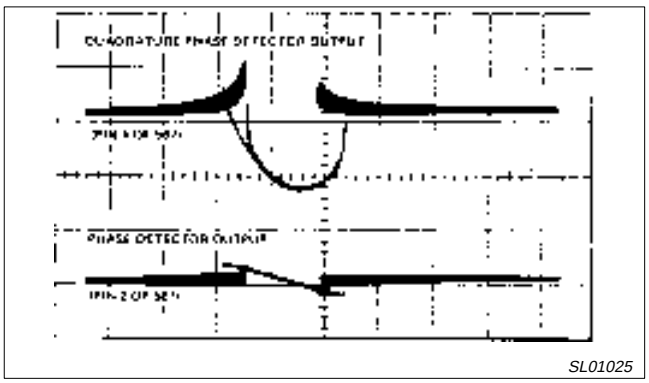

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Figure 15. Quadrature-Phase Detector and Phase Comparator Outputs of the NE567 PLL

Capture and lock range measurements may also be made by sweeping the generator manually through the band of interest. Sweeping must be done very slowly as the edges of the capture range are approached (sweeping toward center frequency) or the lock-up transient delay will cause an error in reading the band edge. Frequency should be read from the generator rather than the loop VCO because the VCO frequency gyrates wildly around the center frequency just before and after lock. Lock and unlock can be readily detected by simultaneously monitoring the input and VCO signals, the DC voltage at the low-pass filter, or the AC beat frequency components at the low-pass filter. The latter are greatly reduced during lock as opposed to frequencies just outside of lock.

FM AND AM DEMODULATION DISTORTION

These measurements are quite straight-forward. The loop is simply set up for FM detection and the test signal is applied to the input. A spectrum analyzer or distortion analyzer (HP333A) can be used to measure distortion at the FM output.

For FM demodulation, the input signal amplitude must be large enough so that lock is not lost at the frequency extremes. The data sheets give the lock (or tracking) range as a function of input signal and the optional range control adjustments. Due to the inherent linearity of the VCOs, it makes little difference whether the FM carrier is at the free-running frequency or offset slightly as long as the tracking range limits are not exceeded.

The faster the FM modulation in relation to the center frequency, the lower the value of the capacitor in the low pass filter must be for

satisfactory tracking. As this value decreases, however, it attenuates the sum frequency component of the phase comparator output less. The demodulated signal will appear to have greater distortion unless this component is filtered out before the distortion is measured.

NATURAL FREQUENCY AND DAMPING

Circuits and mathematical expressions for the natural frequencies and dampings are given in Figure 16 for two first-order low-pass filters. Because of the integrator action of the PLL in converting frequency to phase, the order of the loop always will be one greater than the order of the LPF. Hence, both these first-order LPFs produce a second-order PLL system.

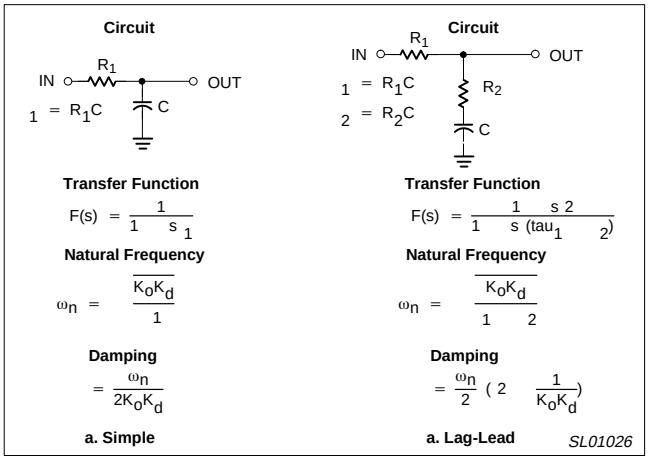


Figure 16. First-Order Low-Pass Filters

The natural frequency (ω_n) of a loop in its final circuit configuration can be measured by applying a frequency-modulated signal of the desired amplitude to the loop. Figure 16 shows that the natural frequency is a function of K_d, which is, in turn, a function of input amplitude. As the modulation frequency (ω_m) is increased, the phase relationship between the modulation and recovered sine wave will go through 90° at $\omega_m = \omega_n$ and the output amplitude will peak.

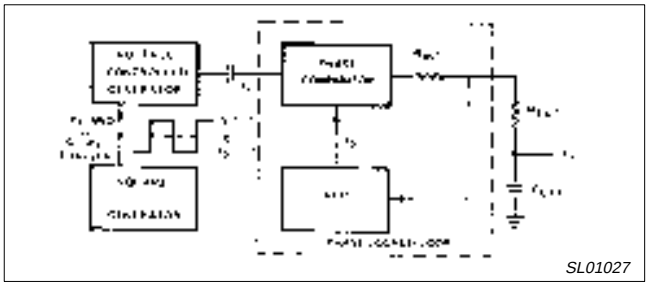


Figure 17. Measurement Setup for Display of PLL Transient Response

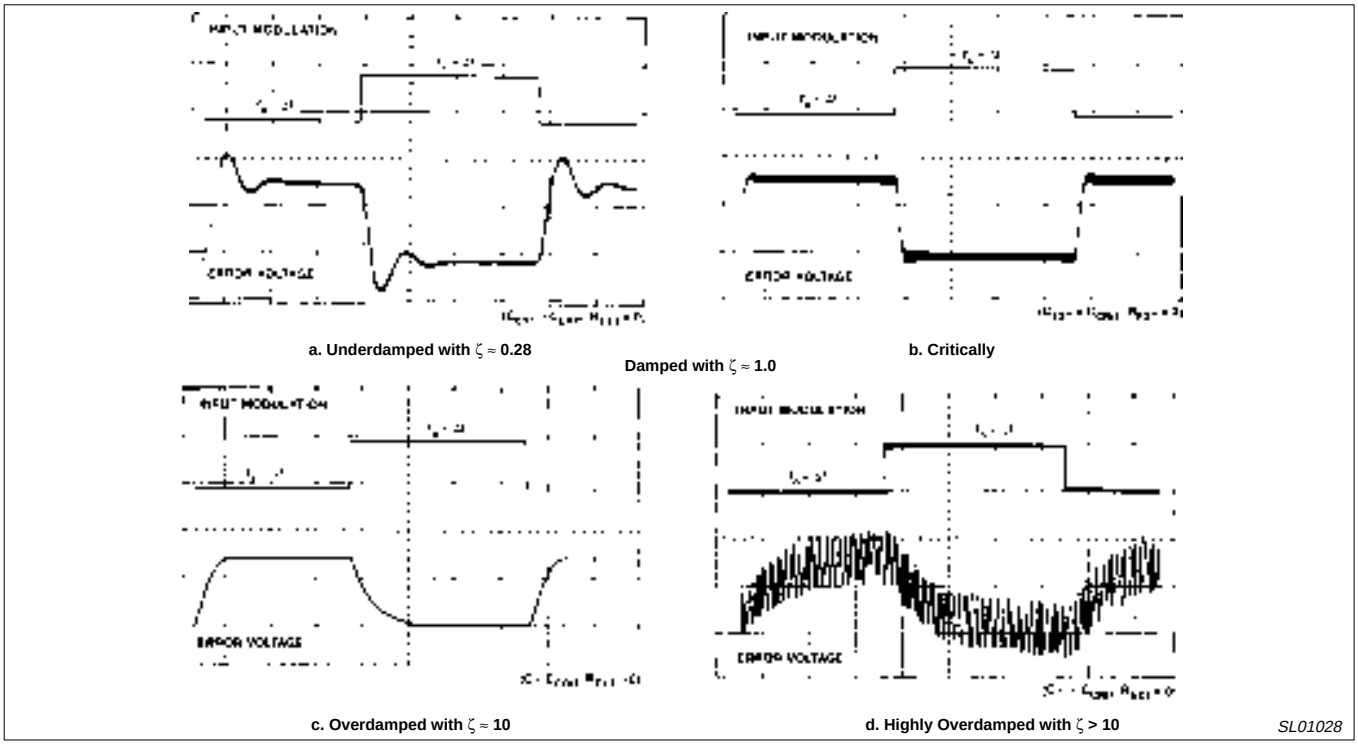
Damping is a function of K_d, K_o, and the lowpass filter. Since K_o and K_d are functions of the free-running frequency and input amplitude, respectively, damping is highly dependent on the particular operating condition of the loop. Damping estimates for the desired operating condition can be made by applying an input signal which is frequency-modulated within the lock range by a square wave. The low-pass filter voltage is then monitored on an oscilloscope which is synchronized to the modulating waveform, as shown in Figure 17. Figure 18 shows typical waveforms displayed. The loop damping can be estimated by comparing the number and magnitude of the overshoots with the graph of Figure 19, which gives the transient phase error due to a step in input frequency.

An expression for calculating the damping for any underdamped second-order system ($\zeta < 1.0$) when the normalized peak overshoot is known is

$$M_p = 1 \quad e^{-\frac{}{1-\ 2}} \qquad (68)$$

Examination of Figure 18 shows that the normalized peak overshoot of the error voltage is approximately 1.4. Using this value for M_p in Equation 68 gives a damping of $\zeta \approx 0.28$.

Another way of estimating damping is to make use of the frequency response plot measured for the natural frequency (ω_n) measurement. For low damping constants, the frequency response measurement peak will be a strong function of damping. For high damping constants, the 3dB down point will give the damping. Figure 19 tabulates some approximate relationships.



a. Underdamped with $\zeta \approx 0.28$

b. Critically Damped with $\zeta \approx 1.0$

c. Overdamped with $\zeta \approx 10$

d. Highly Overdamped with $\zeta > 10$

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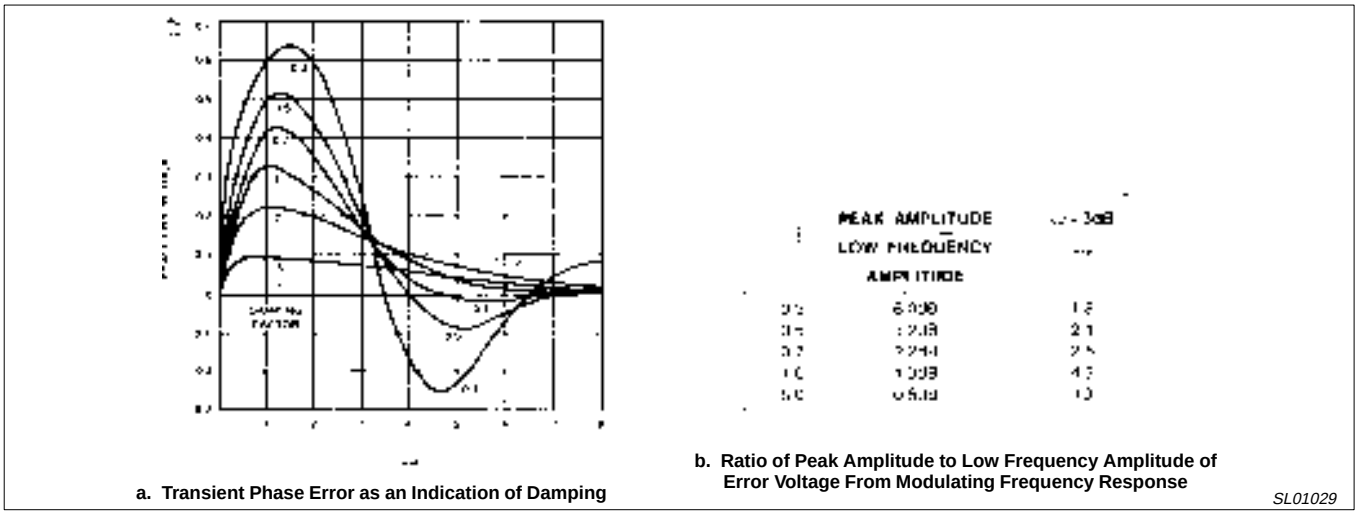
Figure 18. Transient Response of PLL Error Voltage to Square Wave Frequency Modulation for Various Damping Conditions



a. Transient Phase Error as an Indication of Damping

b. Ratio of Peak Amplitude to Low Frequency Amplitude of Error Voltage From Modulating Frequency Response

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Figure 19. Estimating the Damping in a Second-Order PLL

NOISE

The effect of input noise on loop operation is very difficult to predict. Briefly, the input noise components near the center frequency are converted to phase noise. When the phase noise becomes so great that the +905 permissible phse variation is exceeded, the loop drops out of lock or fails to acquire lock. The best techniques is to actually apply the anticipated noise amplitude and badwidth to the input and then perform the capture and lock range measurements as well as perform operating tests with the anticipated input level and modulation deviations. By including a small safety factor in the loop design to compensate for small processing variations, satisfactory operation can be assured.

NOTES

Modeling the PLL AN178

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