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TLC2932

Phase-Locked-Loop Building Block With Analog Voltage-Controlled Oscillator and Phase Frequency Detector

Application Report

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TLC2932

ABSTRACT

The proper usage of the TLC2932IPW, basic concepts relating to conventional PLL blocks, and examples based on experimental results are described in this application report. In the design of a high performance PLL circuit, the parameters of the peripheral circuits such as the counter frequency division setting and the loop filter parameters are determined by the application. The fundamentals needed to produce a high performance PLL are discussed, and the VCO, PFD, frequency divider, and loop filter are examined individually and then as a group.

1 Introduction

The TLC2932IPW integrated circuit (IC) contains a voltage-controlled oscillator (VCO) and a phase frequency detector (PFD) for use in phase-locked-loop (PLL) circuit blocks. A standalone PLL circuit can be designed with the addition of an external frequency divider and a loop filter.

Because the on-chip analog VCO has a wide usable lock frequency range and can cover a wide range of frequencies (11 MHz – 50 MHz) previously unavailable, many new applications are now possible. A stable clock output can be achieved with only one external resistor required for the oscillator. The on-chip PFD uses a widely accepted edge-triggered charge pump circuit. The TLC2932IPW is designed for use as clock frequency generator blocks in digital signal processor (DSP) applications involving video where many video signal frequency bands are possible. Refer to the TLC2932 data sheet (SLAS097) for other features.

2 Theory of an Analog Phase-Locked Loop (PLL)

2.1 Overview

A phase-locked loop is a feedback controlled circuit that maintains a constant phase difference between a reference signal and an oscillator output signal.

2.2 General Operation of a PLL

Figure 1 shows a basic block diagram of a PLL. A phase frequency detector compares the phase of the VCO output frequency, f_{osc}, with the phase of a reference signal frequency, f_{ref}. A phase detector output pulse is generated in proportion to that phase difference. This pulse is smoothed by passing it through a loop filter. The resulting dc component is used as the input voltage for controlling the VCO. The output of the VCO, f_{osc}, is fed back to the phase frequency detector input for comparison which in turn controls the VCO oscillating frequency to minimize the phase difference. Therefore, both frequency and phase are made the same, i.e., $f_{osc} = f_{ref}$ and $\theta_{osc} = \theta_{ref}$, such that the phase and frequency of the VCO and the reference signal source are in a locked state.

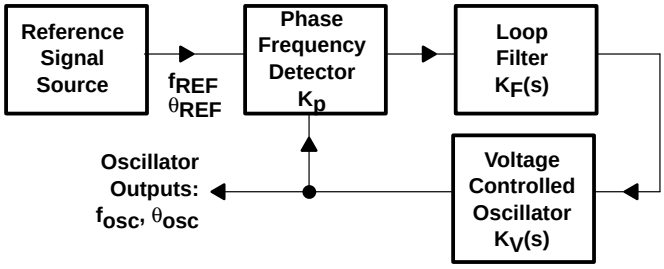


Figure 1. Basic PLL Block Diagram

Therefore, the PLL is a negative feedback circuit which compares the current value to a reference value to make the difference as close to zero as possible.

2.2.1 Analysis of a PLL as a Feedback Control System

An analysis can be performed using the linearized block diagram in Figure 2.

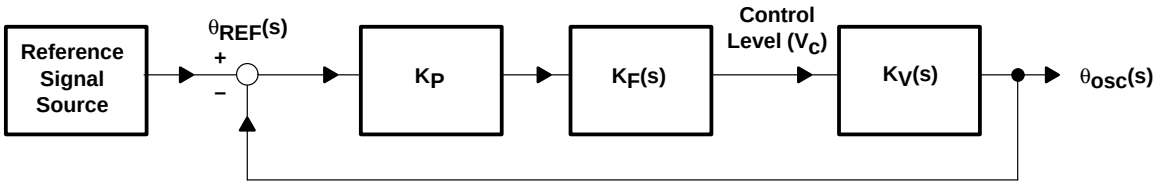


Figure 2. Linearized PLL Block Diagram

The parameters in Figure 2 are defined as follows:

K_P = gain of the phase frequency detector (V/rad)

K_F = transfer function of the loop filter (V/V)

V_c = VCO control level

V_c = VCO control level

s = Laplace variable

Using a Laplace transform, the closed-loop transfer function can be expressed as:

$$\frac{\theta_{osc}(s)}{\theta_{REF}(s)} = \frac{K_P \times K_F(s) \times K_V(s)}{1 + K_P \times K_F(s) \times K_V(s)} = W(s) \quad (1)$$

The VCO transform gain, K_V, is a function of time. Since phase is the time integral of frequency, the gain can be expressed as follows:

$$K_V(s) = \frac{K_V}{s} \quad (2)$$

The phase frequency detector gain is assumed to not to be a function of frequency.

From equation 1 and equation 2

$$W(s) = \frac{K_P \times K_F(s) \times K_V}{s + K_P \times K_F(s) \times K_V} \quad (3)$$

This equation is the general linear transfer function for a PLL.

The PLL has become widely used as a frequency synthesizer by generating frequencies from a single reference signal source such as a crystal oscillator.

Consider the operation of the PLL frequency synthesizer in Figure 3.

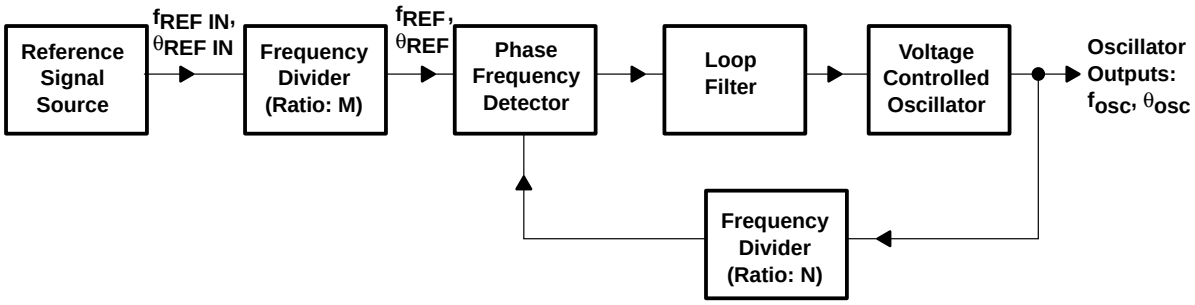


Figure 3. PLL Frequency Synthesizer Block Diagram

Since the signal from the reference signal source is used to generate the desired frequency in a frequency synthesizer, only frequencies at multiples of the reference frequency can be obtained.

The phase frequency detector compares the signal from the *1/N* frequency divider which divides the output signal of the VCO, and the signal from the 1/*M* frequency divider which divides the output signal of the reference signal source, and controls the VCO frequency in such a way so that both frequency and phase are the same.

Therefore, $\frac{f_{refin}}{M} = \frac{f_{osc}}{N}$ (4)

and the oscillating frequency, $f_{osc} = f_{refin} \times \frac{N}{M}$ (5)

The closed-loop transfer function of the PLL in equation 1 can now be considered. If *1/M* and *1/N* frequency dividers are inserted into the block diagram of Figure 3, then Figure 2 becomes Figure 4.

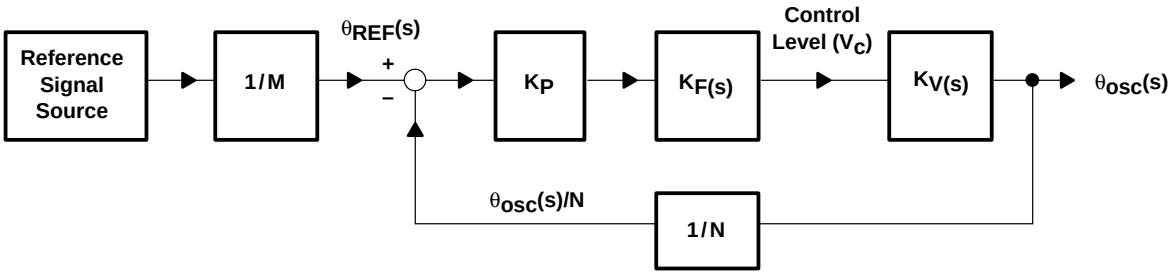


Figure 4. Linearized PLL Frequency Synthesizer Block Diagram

Thus, the closed-loop transfer function can be expressed by the following equation:

$$W(s) = \frac{K_P \times K_F(s) \times K_V}{s + \frac{K_P \times K_F(s) \times K_V}{N}} \quad (6)$$

If the multiplication parameter *N* is set to 1 in equation 6, it becomes equation 3.

In this application report, equation 6 is used as the closed-loop transfer function for the PLL.

From equations 3 and 6, the closed-loop transfer function of the PLL is heavily dependent on the characteristics of the loop filter which is discussed later in this application report.

2.2.2 Definitions

2.2.2.1 Free Running Frequency

The free oscillating frequency of the VCO when it is in an unlocked state is called the free running frequency.

2.2.2.2 Hold-In Range (Lock Range) and Lock-In Range (Capture Range)

When the PLL is in the phase-locked state, the frequency range in which the frequency of the input reference signal, f_{REF}, can slowly be pulled away from the free running frequency of the VCO but still maintain the phase-locked condition is called the hold-in range or lock range. When the PLL is not in the phase-locked state, if the frequency of the input signal, f_{REF}, slowly approaches the free running frequency of the VCO, the frequency range in which the input signal becomes phase-locked is called the lock-in range or capture range.

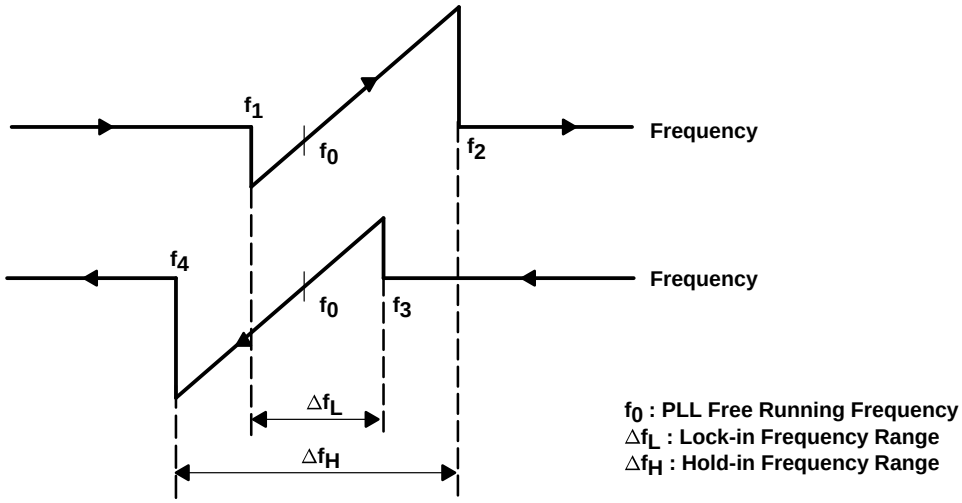


Figure 5. Concept Behind Hold-In Range and Lock-In Range

Referring to the conceptual diagram in Figure 5, if the input signal frequency is increased slowly from a very low frequency not phase-locked to the VCO free running frequency, phase-lock occurs at frequency f_1. If the input signal frequency continually increases, it will pass through the free running frequency and then become unlocked at frequency f_2. Conversely, if the input signal frequency is decreased slowly from a very high frequency not phase-locked to the VCO free running frequency, phase lock occurs at frequency f_3. If the input signal frequency continually increases, it will pass through the free running frequency and the PLL becomes unlocked at frequency f_4. The hold-in range, Δf_H, and lock-in range, Δf_L, can be expressed as the following equations:

$$\Delta f_H = \left(f_2 - f_4\right) \tag{7}$$

$$\Delta f_L = \left(f_3 - f_1\right) \tag{8}$$

Normally, the relationship of $\Delta f_H > \Delta f_L$ exists.

2.2.2.3 Lock-Up Time (Acquisition Time)

The amount of time required for the loop to phase lock is called lock-up time or acquisition time.

2.3 PLL Functional Blocks

2.3.1 Voltage-Controlled Oscillator (VCO)

The VCO is an oscillator circuit with the following characteristics whose output frequency is controlled by a voltage.

- K_V = VCO gain (rad/V/sec) from Section 2.2.1
- Stable with respect to external disturbances (change in voltage, temperature, etc.)
- Control voltage versus oscillating frequency should ideally be linear
- Frequency adjustment should be simple

Because it is extremely difficult to satisfy all these conditions at the same time, a suitable oscillator should be chosen based on the application.

Oscillators that are typically used include the following:

- Crystal oscillator
- LC oscillator
- CR oscillator

For a VCO utilizing any of the above oscillation techniques, many excellent technical books and articles on VCO circuit design should be used.

2.3.2 Phase Detector Operation and Types

A phase detector detects phase differences between two input signals and produces a voltage based on this phase difference.

Phase detectors can be either analog or digital. For analog, representative devices are ring modulators and multipliers which are also called double balanced mixers. For digital, representative devices are OR-gates, ExOR-gates, RS flip-flops, 3-state buffers, and phase frequency detectors.

Only the digital phase detectors are discussed in this application report.

2.3.2.1 OR-Gate Type Phase Detector

The simplest form of digital type phase detectors is the OR-gate type shown in Figure 6(a).

For an OR-gate type phase detector, the output signal duty cycle varies depending on the phase difference as shown in Figure 6(b). Then this output signal is smoothed by an integrator. The resulting output voltage in relation to the phase difference is shown in Figure 6(c).

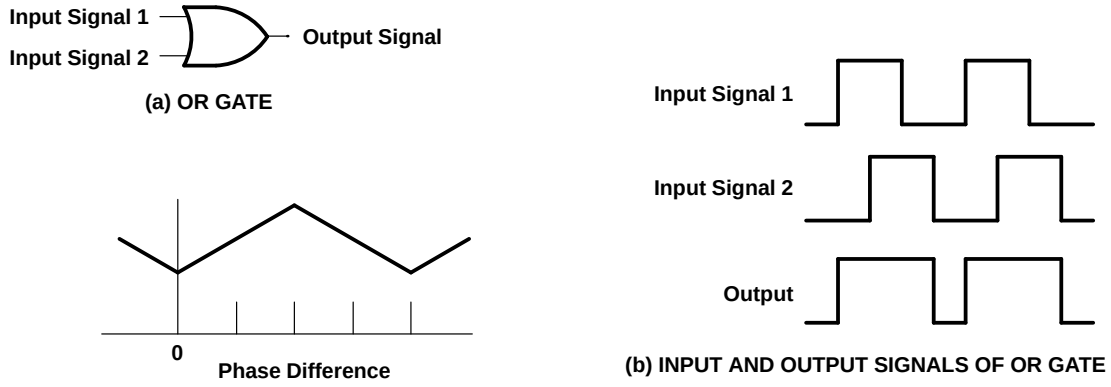
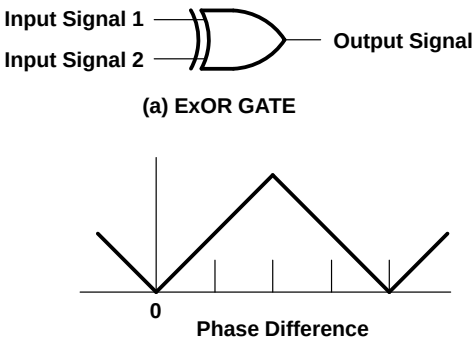


Figure 6. OR-Gate Type Phase Detector

2.3.2.2 ExOR-Gate Type Phase Detector

An ExOR gate phase detector is shown in Figure 7(a).



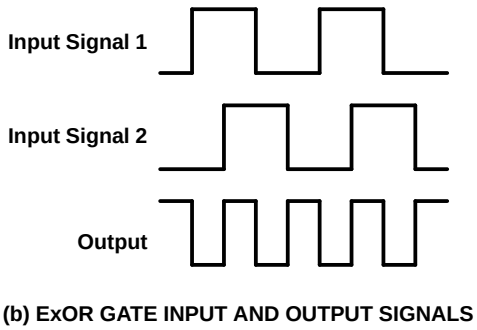


Figure 7. ExOR-Gate Type Phase Detector

For this type of phase detector, the duty cycle of the output signal varies depending on the phase difference as shown in Figure 7(b). This output signal is also smoothed by an integrator. The resulting output voltage in relation to the phase difference is shown in Figure 7(c).

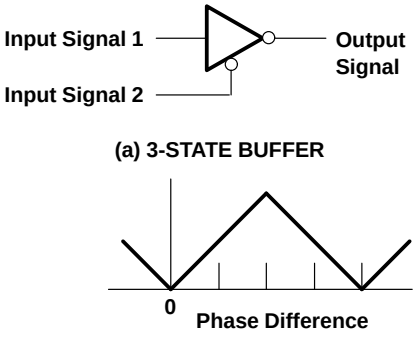
For this ExOR-gate type of phase detector, as compared to an OR-gate type of phase detector, the integrator output signal swings from 0 V to the supply voltage, V_{DD}. Moreover, because the ExOR-gate output frequency is twice that of the OR-gate, the high frequency components are more easily filtered out by the integrator.

However, when using an ExOR-gate as a phase detector, if each input signal duty cycle is not 50%, the output voltage generated from the phase difference does not have acceptable linear characteristics. Therefore, care must be exercised when using this type of phase detector.

2.3.2.3 3-State Buffer Type Phase Detector

A 3-state buffer type phase detector is shown in Figure 8(a).

The 3-state buffer phase detector output characteristic, as shown in Figure 8(c), is basically the same as ExOR gate phase detector. However, when input signal 2 is high, the output is in a high impedance state as shown in Figure 8(b).



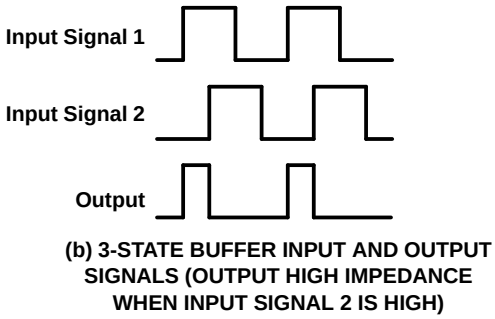


Figure 8. 3-State Buffer Type Phase Detector

2.3.2.4 Reset-Set Flip-Flop Type Phase Detector

A Reset-Set flip-flop phase detector is shown in Figure 9, and the input and output signals are shown in Figure 9(b).

As shown in Figure 9(c), a RS flip-flop type phase detector has twice the comparison range of an ExOR gate type phase detector.

The R-S flip-flop type phase detector can be constructed using only an R-S flip flop. The pulse width of the input signal pulses is small, so a SET-RESET error difference do not cause a significant error. This condition can be solved by inserting AND-gates as shown in Figure 9(a).

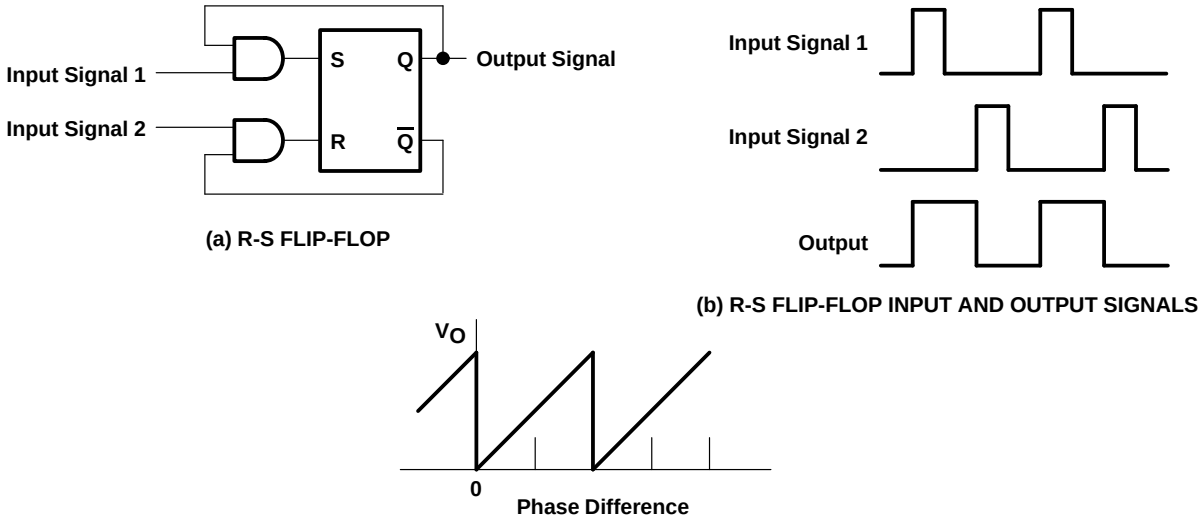


Figure 9. RS Flip-Flop Type Phase Detector

2.3.2.5 Phase Frequency Detector (PFD)

Of the phase detectors currently available, the most commonly used in a PLL is a circuit called a phase frequency detector. Figure 10(a) shows an example of a phase frequency detector.

In Figure 10(b), when the input signal 2 phase lags that of input signal 1, phase detector output D goes high starting from the rising edge of input signal 1 to the rising edge of input signal 2, that is, during the period of time corresponding to a phase difference between inputs 1 and 2, output D goes high. During this same period, output U stays low. When the phase of input 2 leads that of input 1, output D stays low from the rising edge of input 2 to the rising edge of input 1. During that time, U goes high.

When both inputs 1 and 2 have the same phase, both outputs D and U stay low. Depending on the phase detector outputs D and U, the charge pump MOS transistors are turned on and off resulting in output levels of V_{OH}, V_{OL}, or high impedance. So when D is high and U is low, the MOS transistor Q_1 is on and Q_2 is off, therefore, the output level is V_{OH}. When U is high and D is low, Q_2 is on and Q_1 is off, resulting in the output level of V_{OL}. When both D and U are low, Q_1 and Q_2 are both off and the output becomes high impedance.

In this way, the output level is proportional to the phase difference. The output signal characteristic is shown in Figure 10(c).

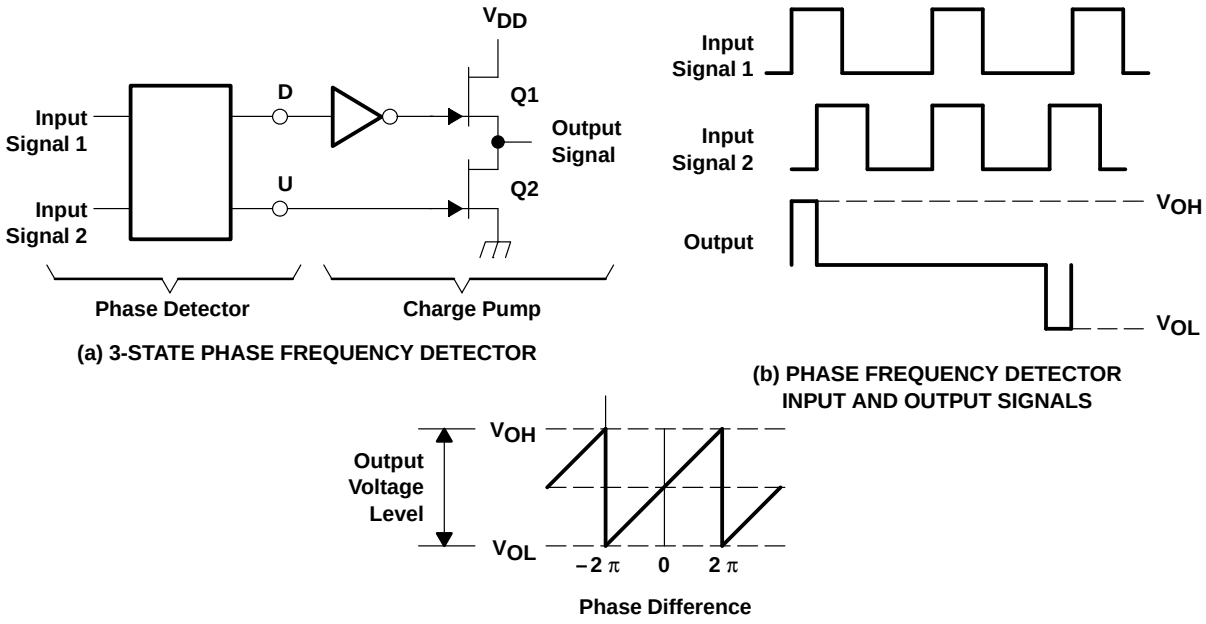


Figure 10. 3-State Phase Frequency Detector

2.4 Loop Filter

The loop filter smooths the output pulses of the phase detector and the resulting dc component is the VCO input. From the closed-loop transfer function (equation 6) obviously the loop filter is very important in determining the characteristics of the PLL response.

Some examples of a loop filter are a lag filter, a lag-lead filter, and an active filter. Among these, the most commonly used are the lag-lead filter and the active filter. For these two filters, the PLL closed loop transfer functions are derived, and design examples for the filter parameters are shown.

2.5 Transfer Function Using a Lag-Lead Filter

First, the lag-lead filter transfer function is derived from Figure 11. If a Laplace transform is taken, then

$$\frac{V_O}{V_D} = K_F(s) = \frac{1 + sC1 \times R2}{1 + sC1(R1 + R2)} = \frac{1 + s\tau_2}{1 + s\left(\tau_1 + \tau_r\right)} \tag{9}$$

Where:

$$\tau_1 = C1 \times R1,\ \tau_2 = C1 \times R2 \tag{10}$$

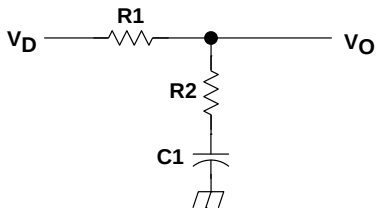


Figure 11. Lag-Lead Filter

By substituting equation 9 into equation 6 and rearranging the terms, the PLL closed-loop transfer function is

$$W(s) = \frac{1 + s\tau_2}{\left\{\left(\tau_1 + \tau_2\right)/K\right\} \times s^2 + \left\{\left(N + K \times \tau_2\right)/(N \times K)\right\} \times s + 1/N} \tag{11}$$

Where:

$$K_P \times K_V = K \tag{12}$$

If this equation is further expanded, it becomes

$$W(s) = W_1(s) + W_2(s) \tag{13}$$

$$= \frac{1}{\left\{\left(\tau_1 + \tau_2\right)/K\right\} \times s^2 + \left\{\left(N + K \times \tau_2\right)/(N \times K)\right\} \times s + 1/N} + \frac{s\tau_2}{\left\{\left(\tau_1 + \tau_2\right)/K\right\} \times s^2 + \left\{\left(N + K \times \tau_2\right)/(N \times K)\right\} \times s + 1/N}$$

The general transfer function for a second order system is shown below

$$G(s) = \frac{1}{\left(1/\omega_n{}^2\right) \times s^2 + \left(2\varsigma/\omega_n\right) \times s + 1} \tag{14}$$

Where:

w_n is the natural angular frequency and z is the damping factor.

If, in equation 15 the right hand side first term is designated as $W_1(s)$ and the second term as $W_2(s)$, then $W_1(s)$ is a second order system as in equation 14 and $W_2(s)$ is a second order lag with gain of τ_2 multiplied by s.

If $W_1(s)$ is equated to equation 14 and the coefficients compared

$$W_1(s) = \frac{1 + s\tau_2}{\left\{\left(\tau_1 + \tau_2\right)/K\right\} \times s^2 + \left\{\left(N + K \times \tau_2\right)/(N \times K)\right\} \times s + 1/N} = \frac{1}{\left(1/\omega_n{}^2\right) \times s^2 + \left(2\varsigma/\omega_n\right) \times s + 1} \tag{15}$$

the following are derived:

$$\omega_n = \sqrt{\frac{K}{N\left(\tau_1 + \tau_2\right)}} \tag{16}$$

$$\varsigma = \frac{1 + K\tau_2}{2\sqrt{N\left(\tau_1 + \tau_2\right) \times K}} = \frac{\omega_n}{2}\left(\tau_2 + \frac{N}{K}\right) \tag{17}$$

Similarly for $W_2(s)$:

$$W_2(s) = \frac{s\tau_2}{\left\{\left(\tau_1 + \tau_2\right)/K\right\} \times s^2 + \left\{\left(N + K \times \tau_2\right)/(N \times K)\right\} \times s + 1/N} = \frac{\left(2\zeta/\omega_n - N/K\right) \times s}{\left(1/{\omega_n}^2\right) \times s^2 + \left(2\zeta/\omega_n\right) \times s + 1} \tag{18}$$

Thus, using a lag-lead filter, the PLL closed-loop transfer function becomes

$$W(s) = W_1(s) + W_2(s) = \frac{1 + (2\zeta/\omega_n - N/K) \times s}{\left(1/\omega_n^2\right) \times s^2 + (2\zeta/\omega_n) \times s + 1} \tag{19}$$

From the above result, design equations for lag-lead filter parameters are derived.

If $\tau_1 = C1 \times R1$ and $\tau_2 = C2 \times R2$ are substituted into equations 16 and 17 respectively and solved for $R1$ and $R2$, the following equations are derived:

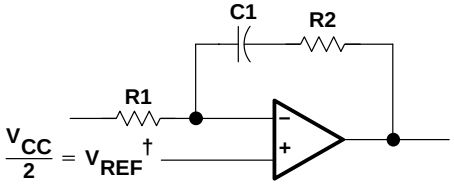
$$R1 = \left(\frac{K}{{\omega_n}^2} \times \frac{1}{N} - \frac{2\zeta}{\omega_n} + \frac{N}{K}\right) \times \frac{1}{C1} \tag{20}$$

$$R2 = \left(\frac{2\zeta}{\omega_n} - \frac{N}{K}\right) \times \frac{1}{C1} \tag{21}$$

2.6 Transfer Function Using an Active Filter

When using an active filter, the PLL closed-loop transfer function and design equation for filter parameters are derived in the same fashion as in Section 2.5.

First, the Laplace transform is taken and the transfer function of an active filter is derived. Figure 12 shows an example of an active filter.



† Voltage used for single ended power supply systems.

Figure 12. Active Filter

The transfer function for the active filter is

$$K_F(s) = \frac{1 + sC1 \times R2}{sC1(R1 + R2)} = \frac{1 + s\tau_2}{s\tau_1} \tag{22}$$

Where:

$$\tau_1 = C1 \times R1 \text{ and } \tau_2 = C1 \times R2 \tag{23}$$

From the PLL closed-loop transfer function, if $K_F(s)$ is substituted into equation 6 and equation 6 is simplified, it becomes

$$W(s) = \frac{1 + s\tau_2}{\left(\tau_1/K\right) \times s^2 + \left(\tau_2/N\right) \times s + 1/N} \tag{24}$$

Where:

$$K_P \times K_V = K \text{ as before.} \tag{25}$$

If this equation is expanded further, it becomes

$$W(s) = W_1(s) + W_2(s) = \frac{1}{\left(\tau_1/K\right) \times s^2 + \left(\tau_2/N\right) \times s + 1/N} + \frac{s\tau_2}{\left(\tau_1/K\right) \times s^2 + \left(\tau_2/N\right) \times s + 1/N} \tag{26}$$

As shown before, second order lag resonators can be expressed as equation 14.

Following the procedure in Section 2.5.

If $W_1(s)$ is equated to equation 14

$$W_1(s) = \frac{1}{\left(\tau_1/K\right) \times s^2 + \left(\tau_2/N\right) \times s + 1/N} = \frac{1}{\left(1/\omega_n{}^2\right) \times s^2 + \left(2\zeta/\omega_n\right) \times s + 1} \tag{27}$$

the following are derived:

$$\omega_n = \sqrt{\frac{K}{N\,\tau_1}} \tag{28}$$

$$\varsigma = \frac{\tau_2}{2N} = \sqrt{\tau_1/(N/K)} = \frac{\omega_n}{2}\,\tau_2 \tag{29}$$

Similarly for $W_2(s)$:

$$W_2(s) = \frac{s\tau_2}{\left(\tau_1/K\right) \times s^2 + \left(\tau_2/N\right) \times s + 1/N} = \frac{\left(2\zeta/\omega_n\right) \times s}{\left(1/\omega_n{}^2\right) \times s^2 + \left(2\zeta/\omega_n\right) \times s + 1} \tag{30}$$

Thus for the active filter, the PLL closed-loop transfer function becomes

$$W(s) = W_1(s) + W_2(s) = \frac{1 + (2\zeta/\omega_n) \times s}{\left(1/\omega_n^2\right) \times s^2 + (2\zeta/\omega_n) \times s + 1} \tag{31}$$

From the above result, the design equation for active filter parameters can be derived.

If $\tau_1 = C1 \times R1$ and $\tau_2 = C1 \times R2$ are substituted into equations 28 and 29 respectively, and solved for *R1* and *R2*, the following two equations are derived:

$$R1 = \frac{K}{\omega_n{}^2} \times \frac{1}{N} \times \frac{1}{C1} \tag{32}$$

$$R2 = \frac{2\zeta}{\omega_n} \times \frac{1}{C1} \tag{33}$$

2.7 General Design Procedures

Based on a PLL step response, the damping factor can be chosen, the natural angular frequency can be evaluated, and the characteristics of response time and relative stability can be examined. For the PLL transfer function in equation 31, the step responses of several cases are shown in Figure 13. As shown, the smaller the ζ value the larger the ringing, and a large ζ value results in little or no ringing. Also, a larger ω_n results in a faster response time.

The step response for a PLL using an active filter as a loop filter is shown in Figure 13. When a passive lag-lead filter is used, if the condition $\omega_n << K/N$ is met for equation 19, the step response is similar to the step response shown.

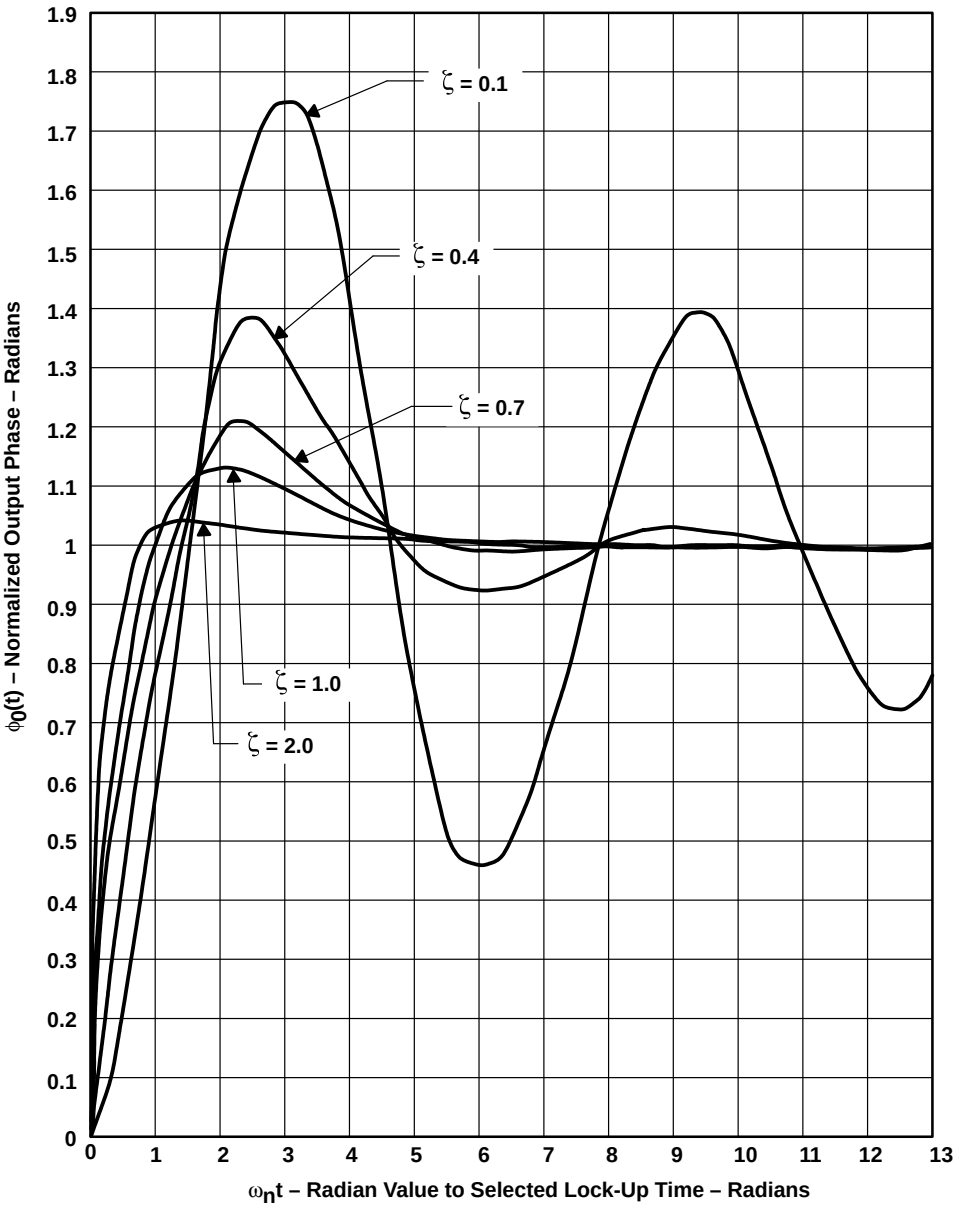


Figure 13. PLL Step Response Using the Active Filter in Figure 17

To design a PLL system, ζ is selected first. Then from the step response characteristic, the value of $\omega_n t$, at which the response is decayed to within 5% of the final value, is found. Then $\omega_n t$ is divided by the desired lock-up time, t_S, to determine ω_n. The following steps should be followed.

1. ζ is a measure of stability. and usually ζ is selected to be between value of 0.6 to 0.8.
2. Assume ζ is selected to be a value of 0.7.
3. The value of $\omega_n t$ from the step response characteristic is determined to be 4.5 for response settling within 5%.
4. Lock-up time, t_S, is determined by system requirements.
5. The PLL natural angular frequency, ω_n, is

$$\omega_n = \frac{\omega_n \tau}{t_s} = \frac{4.5}{t_s} \ (rad/sec) \quad (34)$$

This criterion varies depending on the system application. It is appropriate to pick the natural frequency ($f_n = \omega_n/2\pi$) to be one tenth to one hundredth of the reference frequency of the phase frequency detector.

6. The frequency division ratio is determined from the reference frequency and the desired frequency according to equation 5.
7. Determine the VCO gain parameter, K_V. An example of a VCO oscillating frequency characteristic is shown in Figure 14.

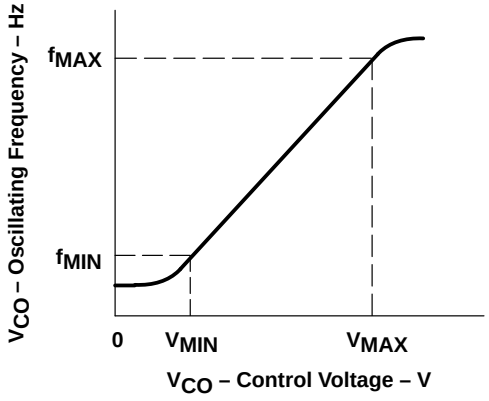


Figure 14. VCO Oscillating Frequency Characteristic

From the oscillating frequency characteristic of Figure 14, the VCO gain can be determined using the following equation:

$$K_V = \frac{f_{MAX} - f_{MIN}}{V_{MAX} - V_{MIN}} \times 2\pi \quad [rad/sec/V] \quad (35)$$

Where:

f_{MAX} = maximum frequency at which the linearity of the oscillating frequency versus the VCO control voltage can be maintained.

f_{MIN} = minimum frequency at which the linearity of the oscillating frequency versus the VCO control voltage can be maintained.

V_{MAX} = control voltage at which the VCO oscillating frequency is f_{MAX}

V_{MIN} = control voltage at which the VCO oscillating frequency is f_{MIN}

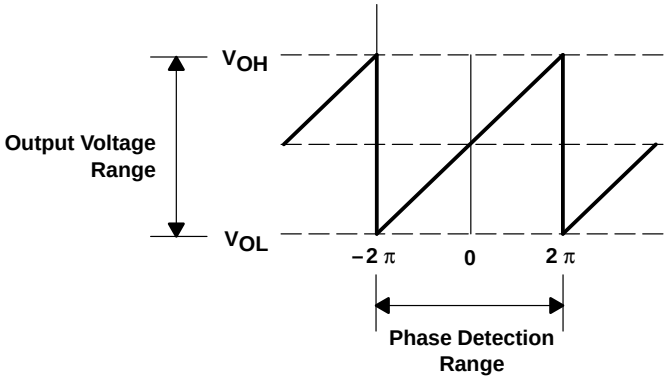


Figure 15. Phase Frequency Detector Output Characteristic

8. Determine the phase detector gain parameter, K_P

   Based on the phase frequency detector output characteristic in Figure 15, the phase detector gain can be determined from equation 34.

$$K_P = \frac{V_{OH} - V_{OL}}{4\pi} \quad [V/rad] \tag{36}$$

   Where:

   V_{OH} = maximum output voltage

   V_{OL} = minimum output voltage

   For other types of phase detectors, the phase detector gain can be determined in the same fashion.

9. Filter parameters can be determined by substituting each of the values determined in steps 1 through 8 into the corresponding equations.

   For the lag-lead filter, substituting the desired values of ω_n, ζ, N, and K into equations 20 and 21, the filter parameters can be determined by choosing an appropriate value for C1.

   For a practical loop filter, a second order lag-lead filter with an additional capacitor C2, as shown in Figure 16, to minimize spurious noise at the VCO input should be used.

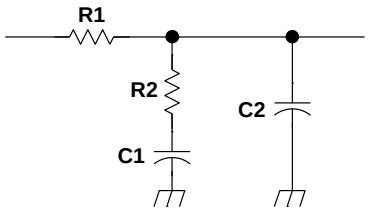


Figure 16. Lag-Lead Filter (With Additional Capacitor)

The value of C2 should be less than or equal to C1/10 to keep C2 from affecting the low-pass filter response while providing adequate noise filtering.

Similarly for the case of an active filter, substituting the desired values of ω_n, ζ, N, and K into equations 32 and 33, the filter parameters can be determined by choosing an appropriate value for C1.

Also when using an active filter as the loop filter, as shown in Figure 17, a second order active filter with one additional capacitor should be used.

The additional capacitor C2 is used for compensating the R2 high frequency response. The cutoff frequency, ω_c, of C2 and R2 should be chosen to be ten times that of the natural frequency, ω_n, of the PLL.

$$\omega_c = \frac{1}{(C2 \times R2)} \cong 10\omega_n \tag{37}$$

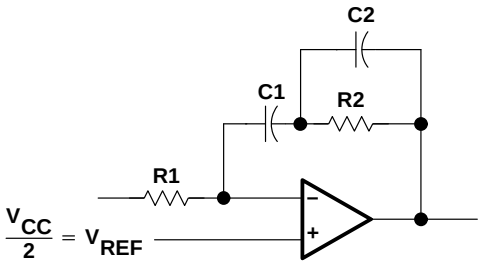


Figure 17. Active Filter (With Additional Capacitor)

2.8 Frequency Division

When given an input signal with frequency f, a circuit that generates a f/N (N an integer) signal synchronized to the input signal is called a frequency divider. Usually frequency dividers use programmable counters like the one shown in Figure 18 (programmable meaning that the frequency divide ratio N can be changed and controlled externally).

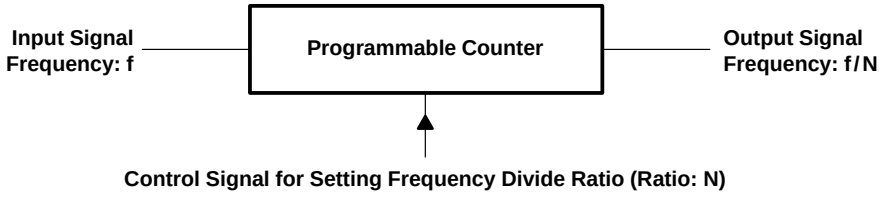


Figure 18. Programmable Counter

The construction of a PLL frequency divider using a programmable counter, and the prescaler and pulse swallow methods (2s modulus prescaler method) are discussed in the following sections.

2.8.1 Prescaler Method

If the frequency, f, of an input signal is too high, a divide can be added using an additional programmable counter in the feedback path. As shown in Figure 19, the frequency can be divided before the programmable counter using a fixed frequency divider (prescaler) operating at high speed, this lowers the input frequency to the programmable counter. This method is called the prescaler method.

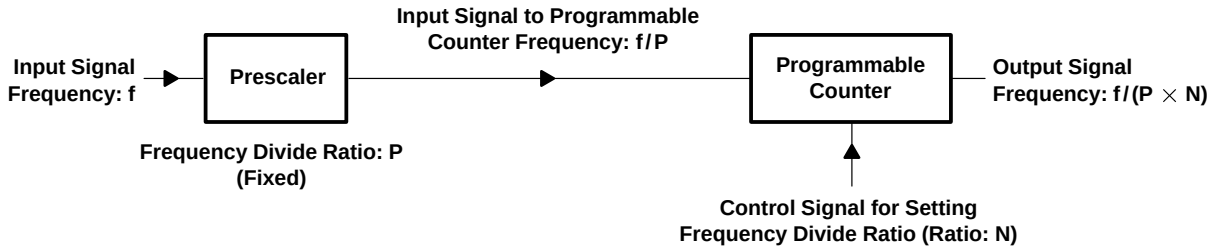


Figure 19. Prescaler Method

The prescaler frequency dividing ratio is fixed. As shown in Figure 19, if the prescaler frequency divide ratio is P and the programmable counter frequency dividing ratio is N, then the total frequency divide ratio becomes P $\times$ N. As shown in Figure 20, if the frequency dividing ratios M and N of the programmable counters are changed, the VCO oscillating frequency is changed in steps of P/M times the phase-reference frequency. Thus the channel space (frequency resolution) becomes $f_{REF} \times P/M$. The PLL f_{REF} should be chosen to be M/P of the channel space. Thus, if f_{REF} is low, the loop-filter time parameters must be designed to be large with respect to f_{REF}; however, the lock-up time can become too large for the application. Noise effects must be considered as well.

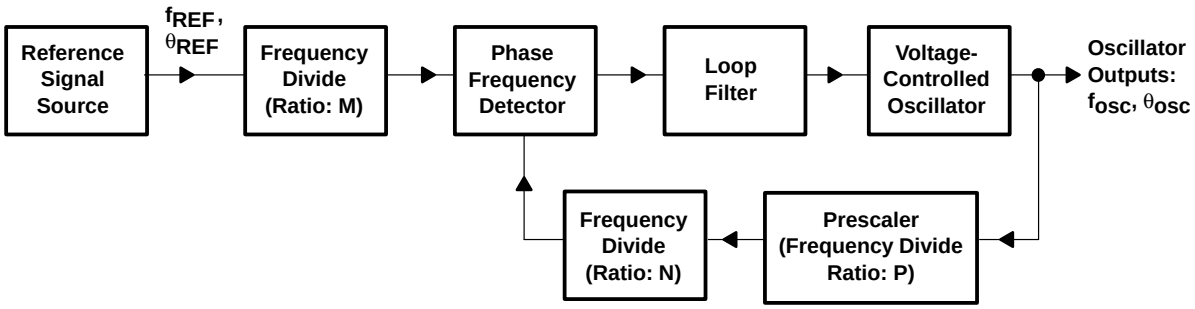


Figure 20. PLL Synthesizer Using Prescaler

2.8.2 Pulse Swallow Method (2s Modulus Prescaler Method)

When the channel space is equal to 1/M of the reference frequency, f_{REF}, the technique is called the pulse swallow method. This method uses a prescaler whose frequency divide ratio can be changed by a control signal as shown in Figure 21.

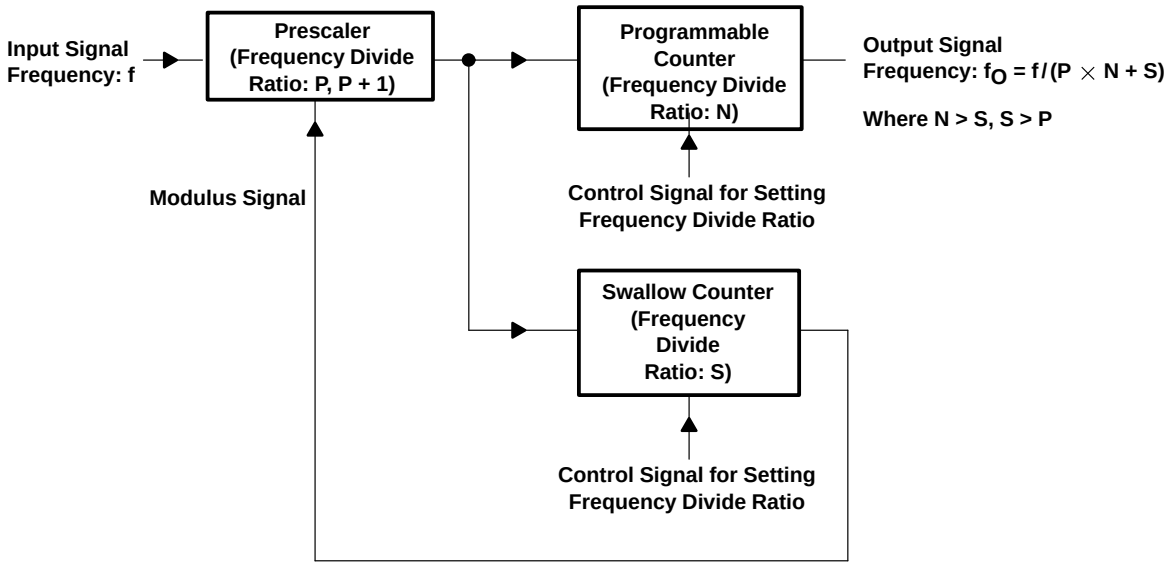


Figure 21. Pulse Swallow Method (2s Modulus Prescaler Method)

The prescaler frequency divide ratio is P or P+1. The counter consists of a programmable counter and a swallow counter which is used to control the prescaler. The frequency divide ratios are N and S respectively.

When the swallow counter is operating, the prescaler frequency divide ratio is P+1. The programmable counter and the swallow counter operate in parallel with the condition N > S. The swallow counter counts up to S and then generates a modulus signal to switch the prescaler. Then the prescaler's frequency divide ratio becomes P.

Thus, during the time period in which the swallow counter is dividing the frequency while counting up to *S* (time period S/N), the total frequency divide ratio is (P+1) × N. During the remaining time period, N–S, in which the programmable counter divides the frequency [time period (N–S)/N], the total frequency divide ratio is $P \times N$. Now the output signal frequency can be expressed by the following equation:

$$f_O = f/(P \times N + S) \tag{38}$$

By examining the actual operation of the PLL shown in Figure 22 and equation 38, P is the coefficient for *N* but not for *S*. Thus, each time the value of *S* changes, the frequency only changes by f_{REF}/M. By using the pulse swallow method and a prescaler, a channel space of f_{REF}/M can be obtained.

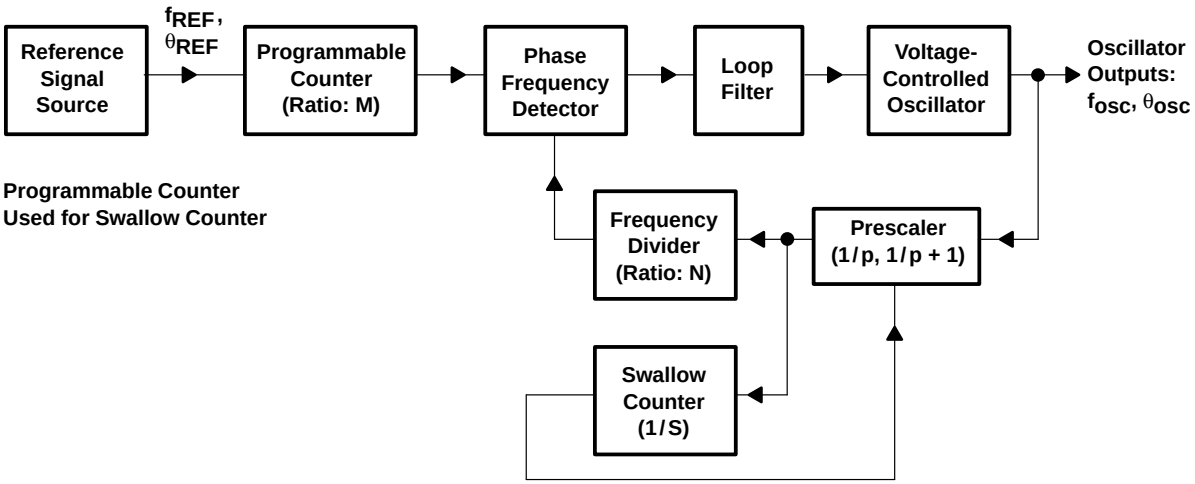


Figure 22. PLL Frequency Synthesizer Based on Pulse Swallow Method

Many variations exist by combining frequency dividers. A specific frequency divider technique can be adopted according to the application.

3 TLC2932IPW

3.1 Overview

The TLC2932IPW can be used for designing high performance PLLs and consists of a voltage controlled oscillator (VCO) operating at up to 50 MHz and an edge detection type phase frequency detector (PFD).

In the design of a PLL, the VCO lock range is determined by the value of a single external bias resistor. In addition, by using the inhibit function, the VCO can be turned off to reduce power dissipation. By switching the VCO output select terminal externally, the output frequency can be divided in half. Thus, lower frequencies can be produced and a 50% duty cycle can be achieved.

With the on-chip charge pump, the PFD detects the phase difference between the rising edges of an external input signal and a phase-reference signal from a reference signal source. Also the PFD output can be controlled externally by the input state to a high impedance output.

The design of a TLC2932IPW system, calculations of loop filters, layout considerations, and input-output protection circuits are explained in the following sections.

3.2 Voltage-Controlled Oscillator (VCO)

The TLC2932IPW VCO has the following special features:

- The VCO only requires one external bias resistor for oscillation and for setting the VCO variable oscillating frequency range. As shown in Figure 23, the possible lock frequency range is from 22 MHz to 50 MHz. The range of possible settings for bias resistance is 1.5 kΩ to 3.3 kΩ.

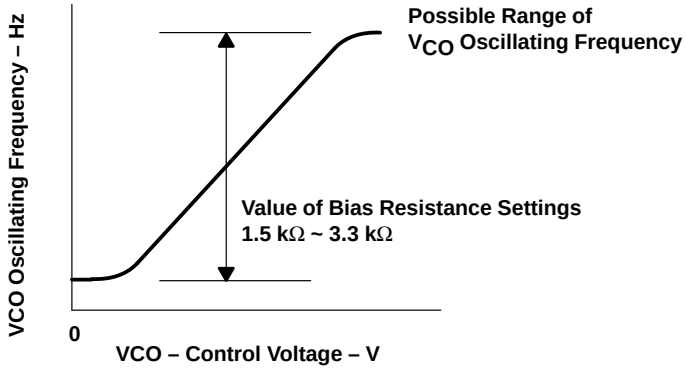


Figure 23. Setting the VCO Oscillating Frequency

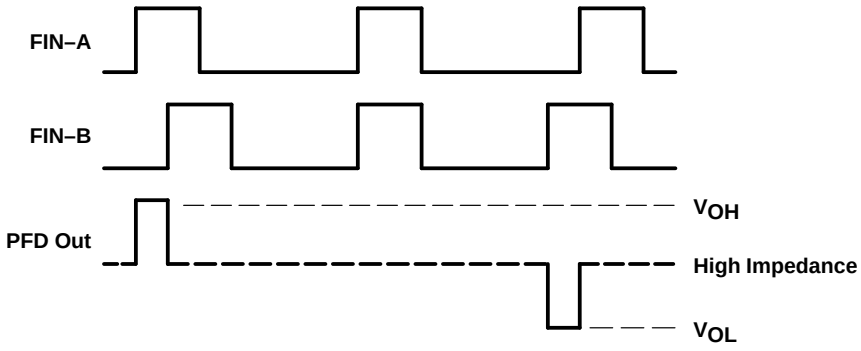
- By switching the VCO select terminal externally, the output frequency can be divided in half to produce a lower frequency; moreover, a duty cycle of 50% is possible. By using this function, the possible frequency range is extended to 11 MHz. Video applications at 14.31818 MHz are possible.
- TLC2932IPW VCO has an inhibit function that is controlled externally
  - The output waveform can be initialized
  - Power dissipation during power down can be reduced

For detailed specifications, refer to the TLC2932 data sheet.

3.3 Phase Frequency Detector (PFD)

TLC2932IPW PFD has the following special features:

- The PFD is a high speed edge triggered type with charge pump. As shown in Figure 24, the difference between the rising edges of two input signal frequencies can be detected.
- Depending on the external controller, the PFD output
  - Can be placed in a high impedance state
  - Is static when put in the power down mode



FIN–A: Phase-reference frequency input from reference signal source
FIN–B: External input frequency

Figure 24. Timing of PFD Operation

3.4 Loop Filter

The loop filter design shown is based on the design equations for loop filter parameters derived in Sections 2.5. and 2.6.

Figure 25 shows a design based on the block diagram of a PLL synthesizer using the prescaler method.

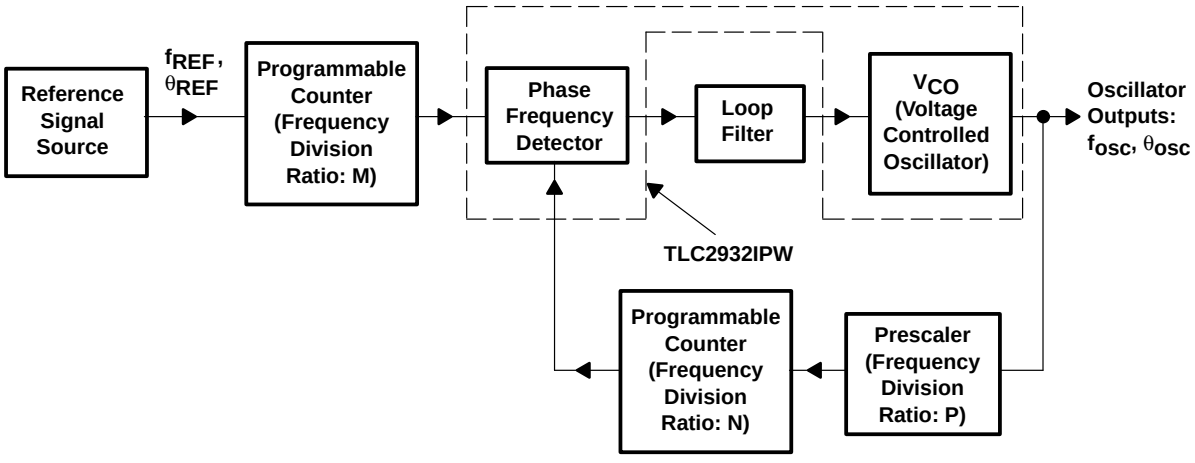


Figure 25. Block Diagram of PLL Synthesizer Using the Prescaler Method

3.5 Setting System Parameters

3.5.1 Setting the Phase Reference Frequency and Output Frequency from a Reference Signal Source

Each frequency is set to the values shown in Table 1. A 14.31818-MHz crystal is used as the reference signal source. This frequency is divided by 910 so that it can be used as the phase reference frequency. Then, the VCO output signal is 14.31818 MHz.

Table 1. Frequency Settings

REFERENCE SIGNAL SOURCE	SYMBOL	VALUE	UNIT
Oscillating frequency	f_{REF}	14.31818	MHz
Phase reference frequency	f_{ref}/M	14.31818/910	MHz
Output frequency	f_{osc}	14.31818	MHz

3.5.2 Setting the Frequency Division Ratios of the Programmable Counter and Prescaler

Using the settings in Table 1, the frequency division ratios of the programmable counter and prescaler can be determined. However, this time the design proceeds based on the settings in Table 2. In practice, the frequency division ratio for the prescaler is based on the frequency operating range of the programmable counter input signal.

Table 2. Settings for Frequency Division Ratios of the Programmable Counters and Prescaler

NAME	PARAMETER	VALUE
Programmable counter (Phase reference frequency side)	M	910
Programmable counter	N	455
Prescaler	P	2

Therefore, the total frequency division ratio becomes $P \times N = 910$.

3.5.3 Setting the Lock-Up Time

The required lock-up time is 2 ms which is the time it takes for the phase to lock and is dependent on system requirements.

3.5.4 Determining the Damping factor, ζ

The damping factor, ζ, is chosen to be 0.7.

3.5.5 Calculating the PLL Natural Angular Frequency, ω_n

For $\zeta = 0.7$ and from equation 34, ω_n is calculated to be

$$\omega_n = \frac{\omega_n \tau}{t} = \frac{4.5}{2 \times 10^{-3}} = 2250 \ (rad/sec)$$

3.5.6 Calculating VCO Gain, K_V

Figure 26 shows an example of the oscillating frequency characteristic of the TLC2932 internal VCO. The VCO gain is calculated from a characteristic curve in the data sheet. By switching the SELECT terminal, the output frequency is divided in half and the resulting characteristic curve is shown in Figure 26.

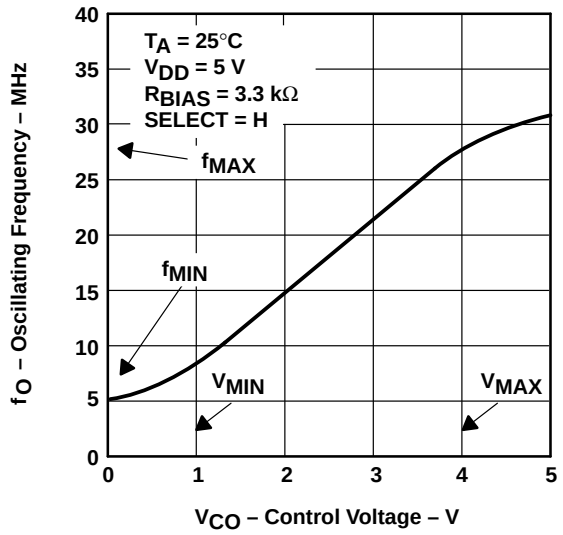


Figure 26. VCO Oscillating Frequency Characteristic

The VCO gain, K_V, from equation 35 is

$$K_V = \frac{f_{MAX} - f_{MIN}}{V_{MAX} - V_{MIN}} \times 2\pi = \frac{(27.5 - 7) \times 10^6}{4 - 1} \times 2\pi \cong 41 \times 10^6 \, [rad/sec/V] \quad (39)$$

3.5.7 Calculating PFD Gain, K_P

The PFD output characteristic is shown in Figure 15. By substituting the values obtained from the data sheet into equation 36, the PFD gain is calculated to be

$$K_P \cong 0.34 \, [V/rad] \quad (40)$$

The design and circuit specifications mentioned above are listed in Tables 3 and 4.

Table 3. PLL Design Specifications

DESIGN SPECIFICATIONS			
NAME	**SYMBOL**	**VALUE**	**UNIT**
PLL damping factor	ζ	0.7	
Radian value to selected lock-up time	$\omega_n t$	4.5	rad
Lock-up time	t	0.002	s
Desired output frequency	f_{osc}	14.318180	MHz
Phase reference frequency	f_{REF}	15734.26374	Hz

Table 4. PLL Circuit Specifications (SELECT Terminal = H)

CIRCUIT SPECIFICATIONS (V_{DD} = 5 V, R_{BIAS} = 3.3 kΩ, T_A = 25°C)			
NAME	**SYMBOL**	**VALUE**	**UNIT**
VCO frequency range	f_{MAX}	27	MHz
	f_{MIN}	7.5	
VCO control voltage range	V_{MAX}	4	V
	V_{MIN}	1	
Phase detector output level	V_{OH}	4.5	V
	V_{OL}	0.2	
Phase detector range of detection		12.56	rad
Frequency divide ratio	N	910	
PLL natural angular frequency	ω_n	2250	rad/sec

3.5.8 Lag-Lead Filter Case

From the design and circuit specifications above and using the lag-lead filter of Figure 16, C2 is selected to be 1/10 of the C1 value.

The calculations are shown in Table 5. The transfer function gain characteristics and phase characteristics are shown in Figure 27 and the step response is shown in Figure 28.

Table 5. Calculation Example of Lag-Lead Filter Parameters

LAG-LEAD FILTER		
PARAMETER	**VALUE**	**UNIT**
C1	1.00E–0.6	F
R1	2476	Ω
R2	557	Ω
C2	1.00E–07	F

Where C2 = C1 × 1/10

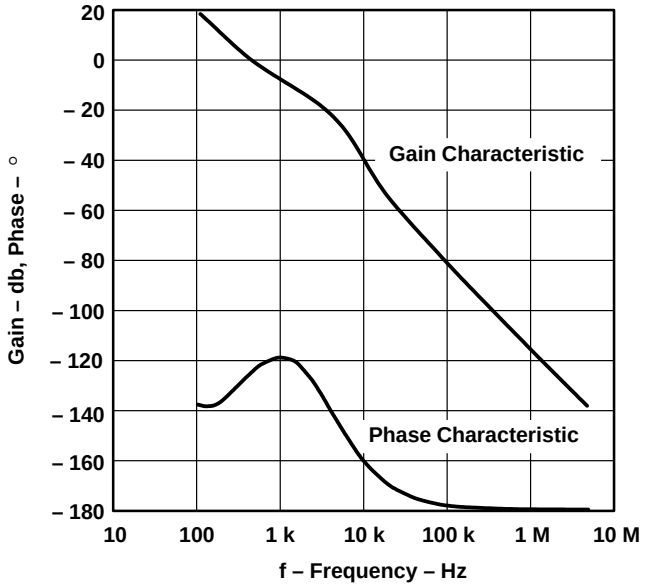


Figure 27. PLL Transfer Function Gain Characteristics and Phase Characteristics (Lag-Lead Filter used as Loop Filter)

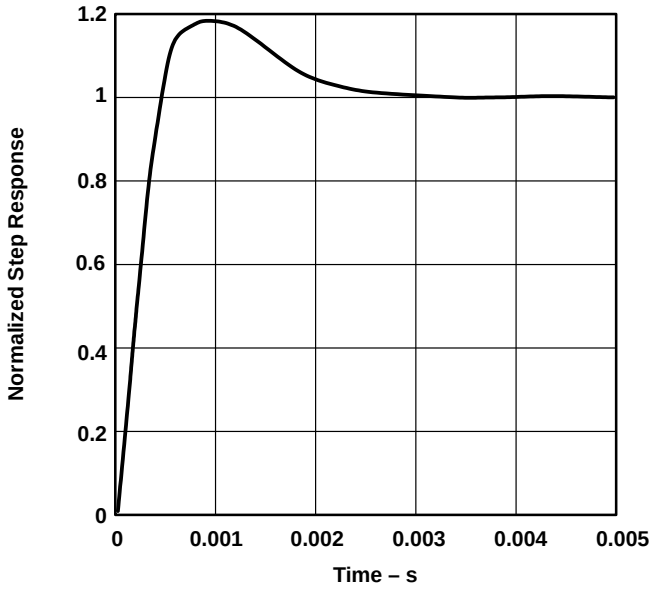


Figure 28. PLL Step Response Characteristic (Lag-Lead Filter used as Loop Filter)

3.5.9 Active Filter Case

The active filter is shown in Figure 17. Each parameter can be calculated using equations 32 and 33. C2 is calculated from equation 37 in Section 2.7.

Table 6 shows an example of these calculations. Figure 29 shows the transfer function gain characteristics and phase characteristics of a PLL using the filter parameters in Table 6. Figure 30 shows the step response of utilizing the filter parameters in Table 6.

Table 6. Calculation Example of Active Filter Parameters

ACTIVE FILTER		
PARAMETER	**VALUE**	**UNIT**
C1	1.00E–6	F
R1	3033	Ω
R2	622	Ω
C2	7.14E–07	F

Where C2 = $1/(10\ \omega_n R2)$

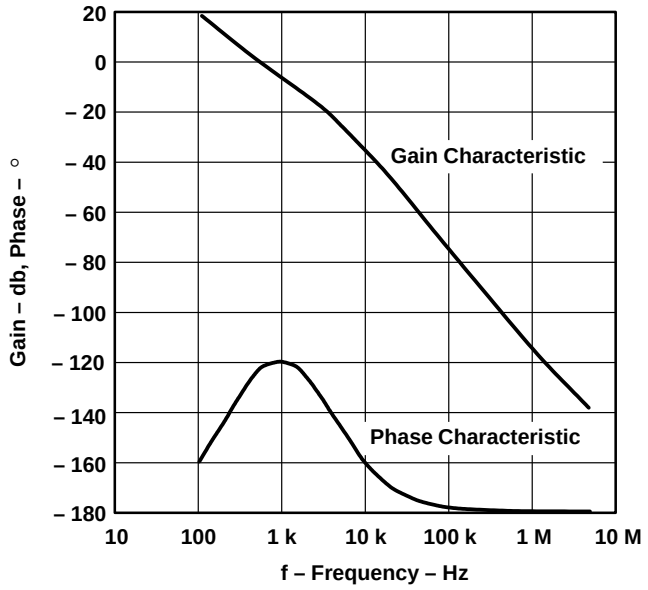


Figure 29. PLL Transfer Function Gain Characteristics and Phase Characteristics (Active Filter used as Loop Filter)

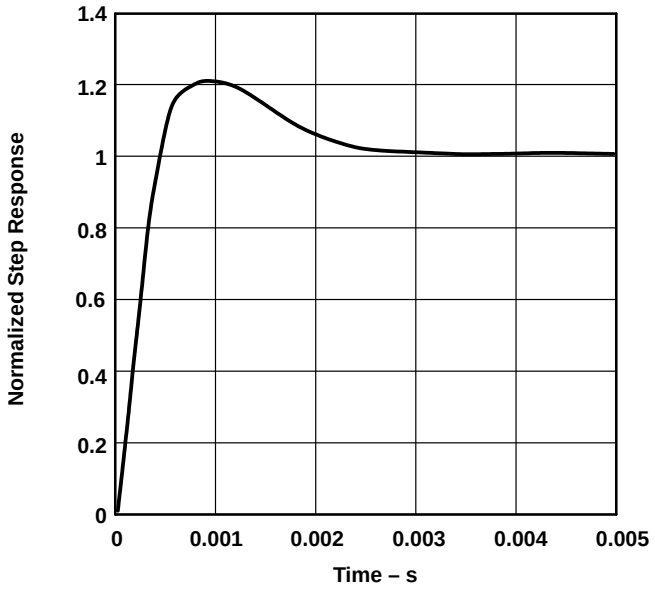


Figure 30. PLL Step Response Characteristic (Active Filter used as Loop Filter)

A basic design example for a PLL loop filter is somewhat of an ideal case. In practice, the PLL characteristics greatly depend on the evaluation board used and the layout of components in the system. Consequently, it is necessary to plan the evaluation board and system carefully.

Section 4, contains the evaluation results of the loop filters.

3.6 Layout Considerations

When designing an evaluation or production board, the following precautions, based on techniques used with high frequency analog circuits must be exercised.

- Depending on the IC socket used, increased circuit resistance, inductance, and capacitance can degrade the performance in some cases. If possible, do not use IC sockets. Direct connection to the board is recommended.
- Extreme care should be exercised with wiring and connections. Casual wiring should be avoided.
- Power supplied to the V_{DD} terminal of the VCO should be separated from the digital portion. Moreover, by inserting high pass capacitors, noise coupling can be avoided as much as possible.
- It is necessary to consider the VCO ground terminal. The analog portion and digital portion must be separated. The analog portion should be connected to a ground plane. The design should avoid the coupling of switching noise from the digital portion.
- The loop filter ground should be connected to analog ground.
- External components (such as the loop filter and high pass capacitors) should be placed as close as possible to the IC.

Layouts and bread boards must be carefully designed to realize the full potential of the TLC2932. These techniques must be used to ensure proper operation of the PLL design.

3.7 Input-Output Protection Circuits

The input and output protection circuits are shown in Table 7.

Table 7. Input-Output Protection Circuits

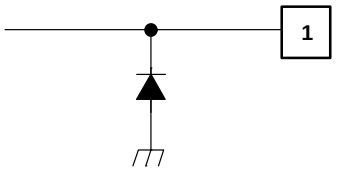
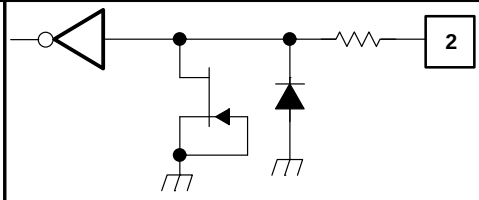
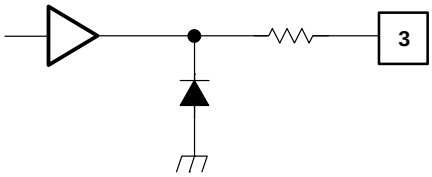
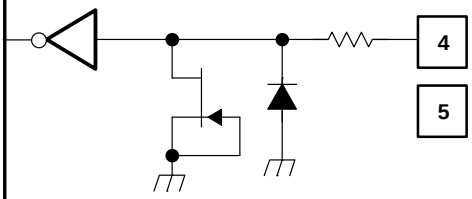
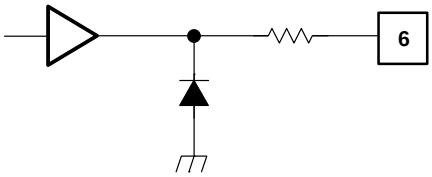
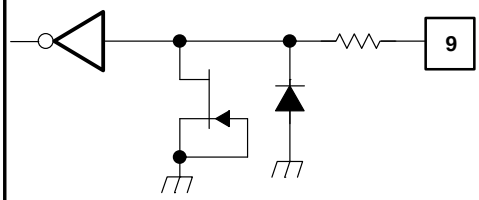
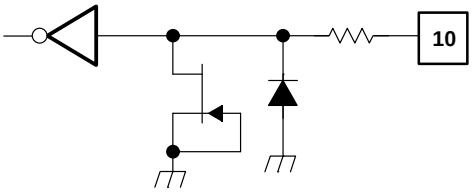
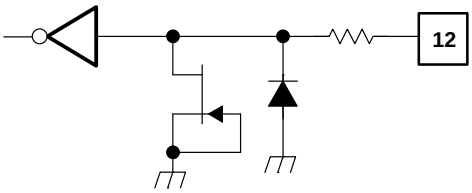
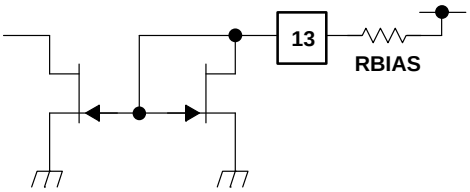
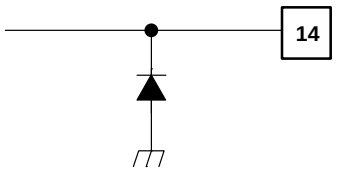
TERMINAL NAME	NO.	CIRCUIT	FUNCTION
LOGIC V_{DD}	1		Voltage supply terminal for internal logic. It is desirable to separate completely from the VCO voltage supply terminal.
SELECT	2		VCO output frequency 1/2 divider select terminal. By controlling this terminal using external logic, the VCO output frequency can be divided in half.
VCO OUT	3		VCO output terminal. During inhibit, this terminal is taken low.
FIN-A,B	4, 5		The two input terminals used for detecting the edge difference of reference frequency, f_{ref}-IN, and external counter's frequency. Usually f_{ref}-IN is connected to the FIN-A terminal and the external counter output frequency is connected to the FIN-B terminal.
PFD OUT	6		The PFD output terminal can be put in high impedance state.
LOGIC GND	7		Internal logic ground terminal.
NC	8		Not connected internally.
PFD INHIBIT	9		The PFD inhibit function control terminal.

Table 7. Input-Output Protection Circuits (Continued)

TERMINAL NAME	TERMINAL NO.	CIRCUIT	FUNCTION
VCO INHIBIT	10		The VCO inhibit function control pin
VCO GND	11		VCO ground terminal
VCO IN	12		The VCO control voltage input terminal usually connected to VCO control voltage from the external loop filter of PLL.
R BIAS	13		The terminal for connecting the bias resistor for setting the VCO oscillating frequency. To provide a bias for the operation of internal VCO and for frequency setting and tuning, a bias resistor is connected between this terminal and the power supply line.
VCO V_{DD}	14		This terminal supplies the supply voltage to the VCO. It is desirable to completely separate this from the logic power terminal.

4 Application Example

4.1 Introduction

An evaluation example using the TLC2932IPW in a PLL application is described in the following sections.

4.2 National Television System Committee (NTSC) Method 4 Frequency Sub-Carrier (fsc), 8 fsc Output Signal Evaluation

Table 8 shows that by combining a phase reference frequency and loop filter, the NTSC method of 4 fsc and 8 fsc output signals can be generated.

The block diagram is shown in Figure 31. Figure 32 shows the circuit for evaluation, using a passive lag-lead filter as the loop filter. This evaluation circuit is based on the conditions stated in number 2 of Table 8.

When an active filter is used, because of additional inversion added to the loop, the phase frequency detector input signal is reversed from that in the passive lag-lead filter case.

Table 8. Evaluation Conditions (V_{DD} = 5 V, T_A = 25°C, R_{BIAS} = 3.3 kΩ)

NO.	PHASE REFERENCE FREQUENCY	OUTPUT FREQUENCY	LOOP FILTER	EVALUATION RESULT
1	fsc (NTSC) = 3.579545 MHz	4 fsc (NTSC) = 14.31818 MHz	Lag-lead and active	Section 4.3
2	HD (NTSC) = 4 fsc/910 ≈ 15.7 kHz	4 fsc (NTSC) = 14.31818 MHz		Section 4.4
3	HD (NTSC) = 4 fsc/910 ≈ 15.7 kHz	8 fsc = 28.63636 MHz		Section 4.5

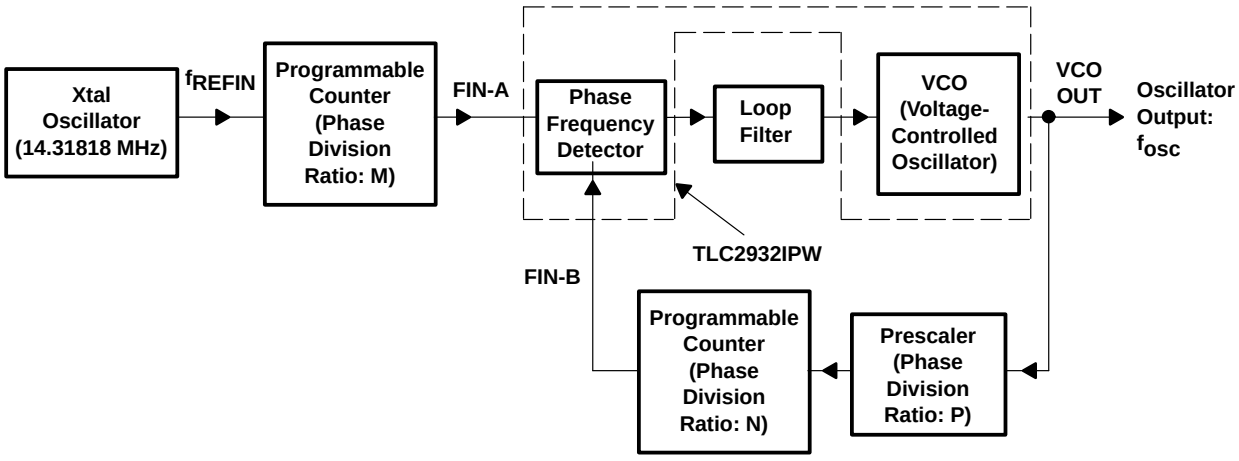


Figure 31. 4 fsc Output Evaluation Block Diagram

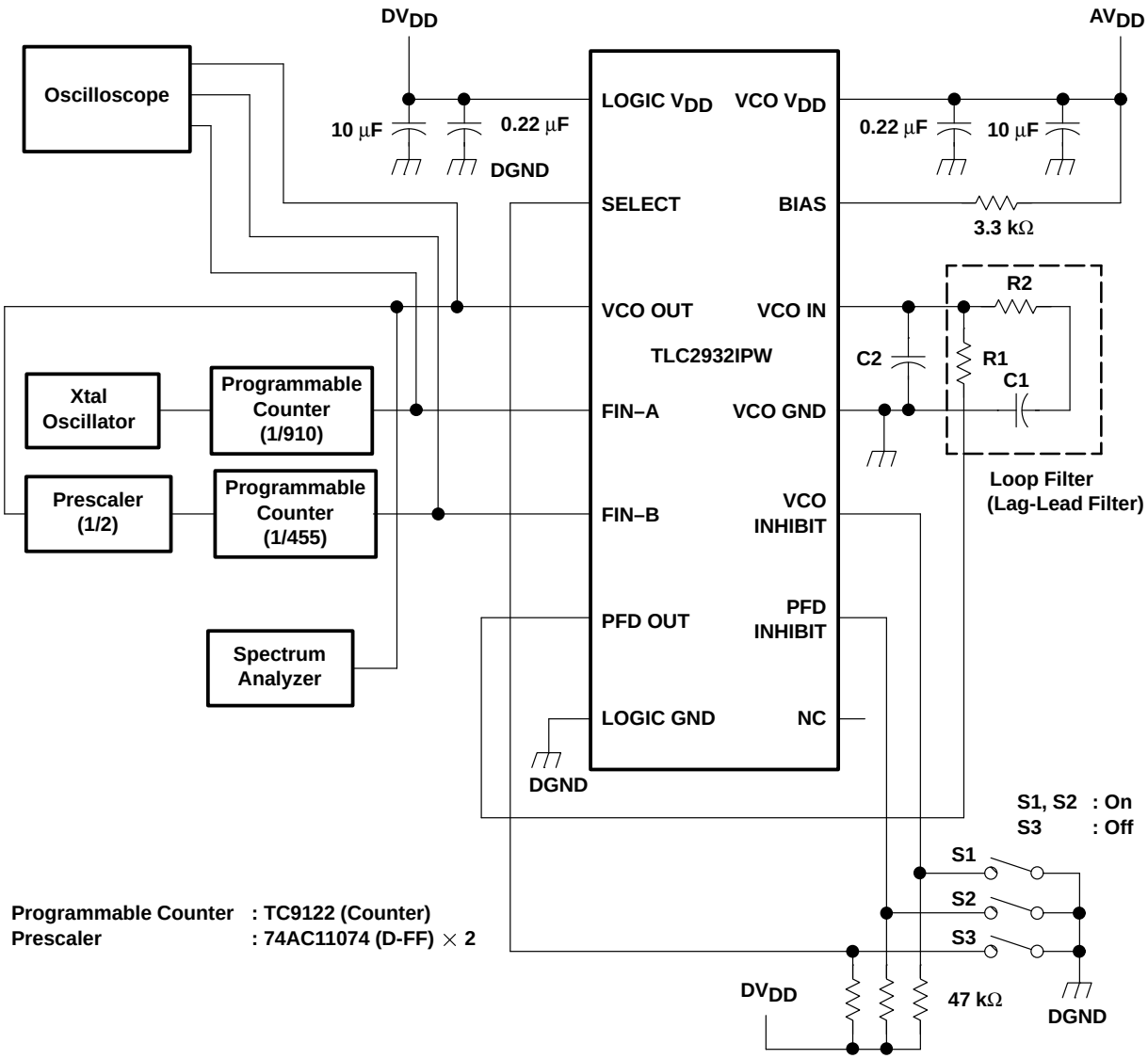


Figure 32. Evaluation Circuit (Based on Number 2 of Table 1) (Lag-Lead Filter Used as Loop Filter)

4.3 Evaluation Results (Phase Reference Frequency = fsc, Output Frequency = 4 fsc)

In this evaluation, the fsc (3.579545 MHz) shown as number 1 in Table 8, is used as the phase reference frequency to generate a 4-fsc (14.31818 MHz) output frequency. The details and results for the cases of using a lag-lead filter and an active filter as the loop filter are described in the following sections.

4.3.1 Programmable Counter and Prescaler Frequency Division Ratio Settings

Based on the evaluation block diagram of Figure 31, the frequency division ratio settings for the programmable counters and prescaler are listed in Table 9.

Table 9. Frequency Division Ratio Settings

FREQUENCY DIVISION RATIO	M	P	N	P × N
Frequency divide value	4	1	4	4

4.3.2 Loop Filter Parameter Settings

From the loop filter design procedures of Sections 2.5 and 2.6, the setting of each parameter is listed in Table 10.

Table 10. Loop Filter Parameter Settings

LOOP FILTER TYPE	C1	R1	R2	C2	CIRCUIT CONSTRUCTION
Lag-lead filter	1 μF	1.6 kΩ	36 Ω	0.1 μF	Figure 16
Active filter	1 μF	1.6 kΩ	36 Ω	0.1 μF	Figure 17

NOTE: The numerical values in Table 3 are the capacitance and resistance closest to the calculated values.

4.3.3 Passive Lag-Lead Filter Used as a Loop Filter

The evaluation results of using a lag-lead filter as the loop filter are illustrated in Figure 33 and Figure 34. Figure 33 shows the individual waveforms as observed from an oscilloscope. Figure 34 shows the output signal measured by a spectrum analyzer.

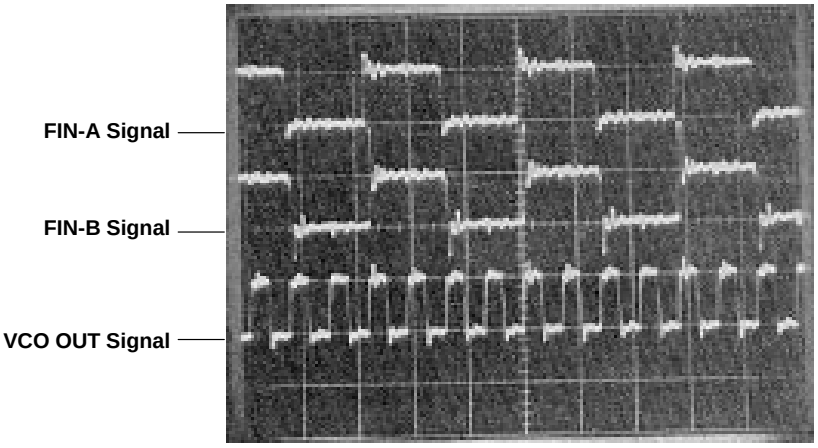


Figure 33. Waveforms Using Passive Lag-Lead Filter (100 ns/div on Horizontal Axis)

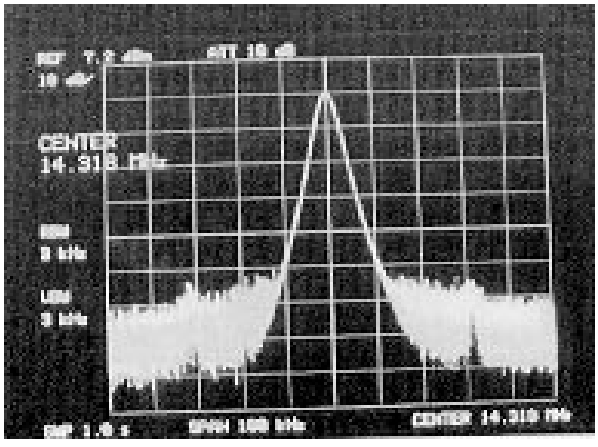


Figure 34. Spectrum of the VCO Output Signal When Using a Passive Lag-Lead Filter (100 kHz/div on Horizontal Axis)

4.3.4 Active Filter Used as a Loop Filter

The evaluation results of using an active filter as the loop filter are illustrated in Figure 35 and Figure 36. Figure 35 shows the individual waveforms as observed from an oscilloscope. Figure 36 shows the output signal measured by a spectrum analyzer.

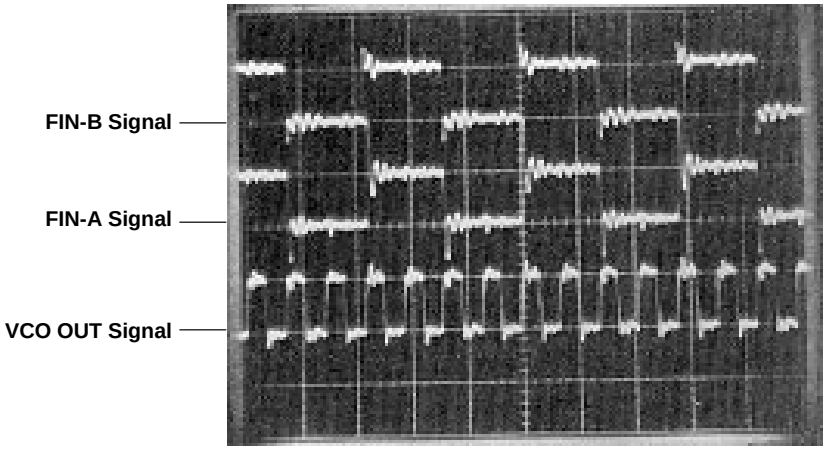


Figure 35. Waveforms Using Active Filter (100 ns/div on Horizontal Axis)

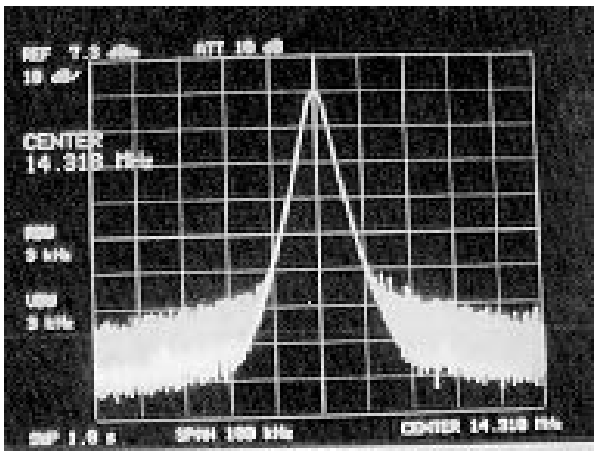


Figure 36. Spectrum of the VCO Output Signal When Using an Active Filter (100 kHz/div on Horizontal Axis)

4.4 Evaluation Results (Phase Reference Frequency = 4 fsc/910, Output Frequency = 4 fsc)

In this evaluation of number 2 in Table 8, fsc/910 (15.7 kHz) is used as the phase reference frequency to generate a 4 fsc (14.31818 MHz) output frequency. The details and results for the cases of using a lag-lead filter and an active filter as the loop filter are described in the following sections.

4.4.1 Programmable Counter and Prescaler Frequency Division Ratio Settings

Based on the evaluation block diagram of Figure 31, the frequency division ratio settings for the programmable counter and prescaler are listed in Table 11.

Table 11. Frequency Division Ratio Settings

FREQUENCY DIVISION RATIO	M	P	N	P×N
Frequency divide value	910	2	455	910

4.4.2 Loop Filter Settings

Following the loop filter design procedures of Sections 5 and 6, the setting of each parameter is listed in Table 12.

Table 12. Loop Filter Parameter Settings

LOOP FILTER	C1	R1	R2	C2	CIRCUIT CONSTRUCTION
Lag-lead filter	1 μF	2.4 kΩ	560 Ω	0.1 μF	Figure 16
Active filter	1 μF	3 kΩ	620 Ω	0.1 μF	Figure 17

NOTE: Numerical values in Table 5 are the capacitance and resistance closest to the calculated values.

4.4.3 Passive Lag-Lead Filter Used as a Loop Filter

Using lag-lead filter as the loop filter, the evaluation results are illustrated in Figure 37 and Figure 38. Figure 37 shows the individual waveforms as observed from an oscilloscope. Figure 38 shows the output signal measured by a spectrum analyzer.

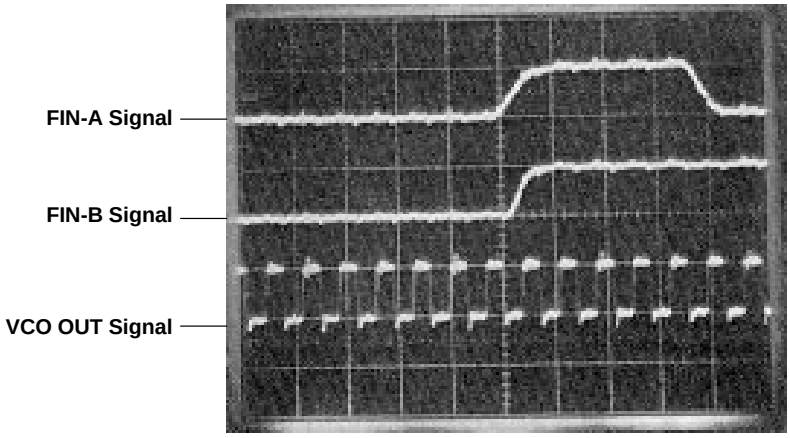


Figure 37. Waveforms Using Passive Lag-Lead Filter (100 ns/div on Horizontal Axis)

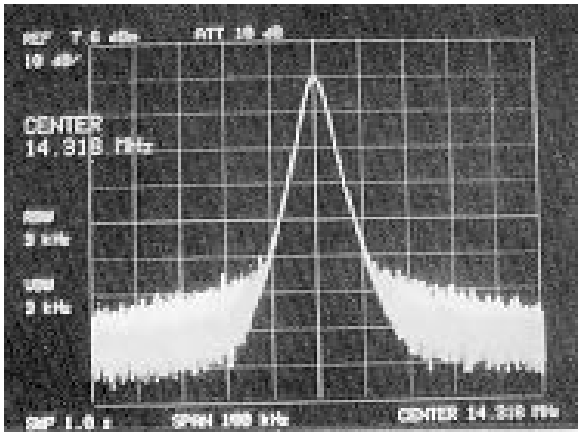


Figure 38. Spectrum of the VCO Output Signal When Using a Passive Lag-Lead Filter (100 kHz/div on Horizontal Axis)

4.4.4 Active Filter Used as a Loop Filter

Using an active filter as the loop filter, the evaluation results are illustrated in Figure 39 and Figure 40. Figure 39 shows the individual waveforms as observed from an oscilloscope. Figure 40 shows the output signal measured by a spectrum analyzer.

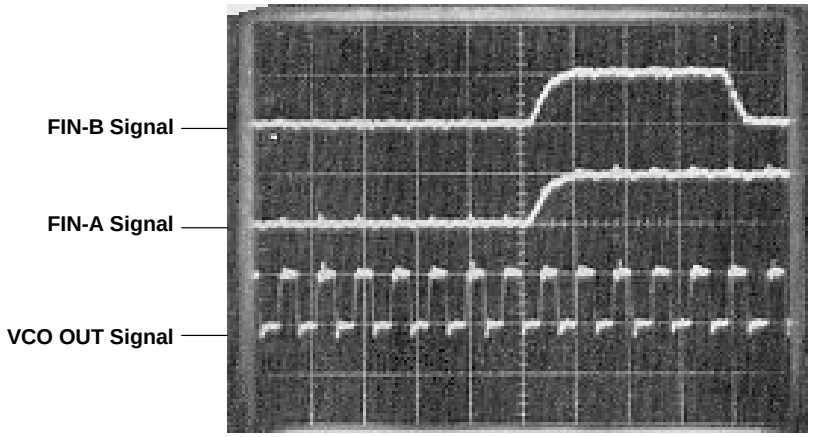


Figure 39. Waveforms Using Active Filter (100 ns/div on Horizontal Axis)

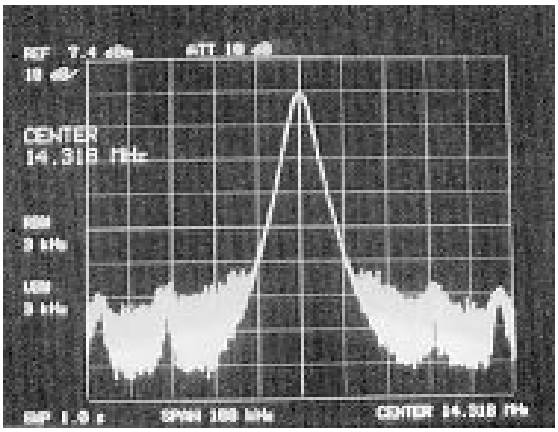


Figure 40. Spectrum of the VCO Output Signal When Using an Active Filter (100 kHz/div on Horizontal Axis)

4.5 Evaluation Results (Phase Reference Frequency = fsc/910, Output Frequency = 8 fsc)

In this evaluation of number 1 in Table 8, fsc (3.579545 kHz) is used as the phase reference frequency to generate a 8 fsc (2 × 14.31818 MHz) output frequency. The details and results for the cases of using a lag-lead filter and an active filter as the loop filter are described in the following sections.

4.5.1 Programmable Counter and Prescaler Frequency Division Ratio Settings

Based on the evaluation block diagram of Figure 31, the frequency division settings for programmable counters and prescaler are listed in Table 13.

Table 13. Frequency Division Ratio Settings

FREQUENCY DIVIDE RATIO	M	P	N	P×N
Frequency dividing value	910	4	455	1820

4.5.2 Loop Filter Settings

Following the loop filter design procedures of Sections 5 and 6, the setting of each parameter is listed in Table 14.

Table 14. Loop Filter Parameter Settings

LOOP FILTER	C1	R1	R2	C2	CIRCUIT CONSTRUCTION
Lag-lead filter	1 μF	2.4 kΩ	560 Ω	0.1 μF	Figure 16
Active Filter	1 μF	3 kΩ	620 Ω	0.1 μF	Figure 17

NOTE: Numerical values in Table 13 are the capacitance and resistance closest to the calculated values.

4.5.3 Passive Lag-Lead Filter Used as a Loop Filter

The evaluation results of using a lag-lead filter as the loop filter are illustrated in Figure 41 and Figure 42. Figure 41 shows the individual waveforms as observed from an oscilloscope. Figure 42 shows the output signal measured by a spectrum analyzer.

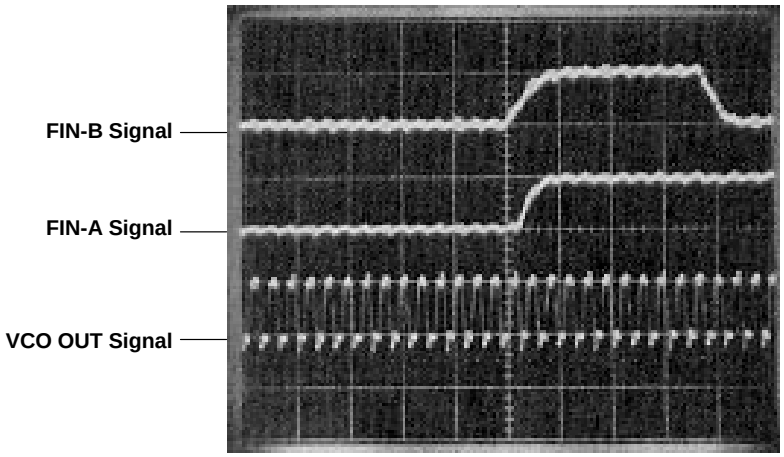


Figure 41. Waveforms Using Passive Lag-Lead Filter (100 ns/div on Horizontal Axis)

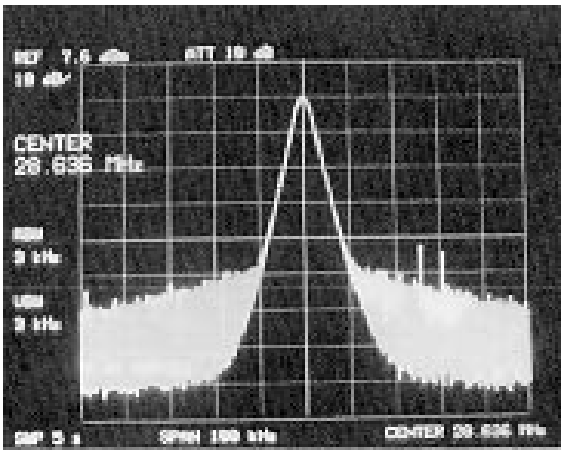


Figure 42. Spectrum of the VCO Output Signal When Using a Passive Lag-Lead Filter (100 kHz/div on Horizontal Axis)

4.5.4 Active Filter Used as a Loop Filter

The evaluation results of using an active filter as the loop filter are illustrated in Figure 43 and Figure 44. Figure 43 shows the individual waveforms as observed from an oscilloscope. Figure 44 shows the output signal measured by a spectrum analyzer.

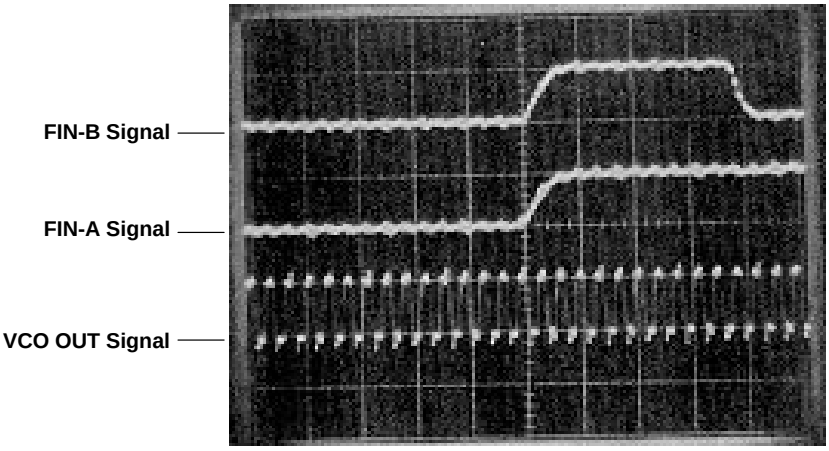


Figure 43. Waveforms Using an Active Filter (100 ns/div on Horizontal Axis)

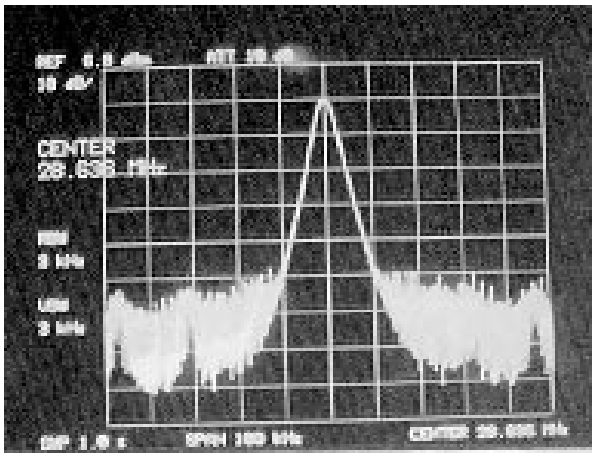


Figure 44. Spectrum of the VCO Output Signal When Using an Active Filter (100 kHz/div on Horizontal Axis)

5 Summary

The evaluation results shown were with the practical resistance and practical capacitance values closest to the calculated values used for the loop filter. The evaluations were carried out with a TLC2932IPW placed in the IC socket on an evaluation board with power supplies, and the BIAS terminal was bypassed directly on the bottom of the socket.

Better results can be achieved however by placing the TLC2932IPW directly on the evaluation board.

5.1 Examples of a PLL Application

The following sections contain PLL application examples.

5.1.1 Generating a 4-fsc NTSC Signal from a NTSC Signal

A NTSC signal horizontal synchronization frequency (f_H) is multiplied by 910 to generate a 4-fsc NTSC signal. Figure 45 shows a block diagram of the PLL.

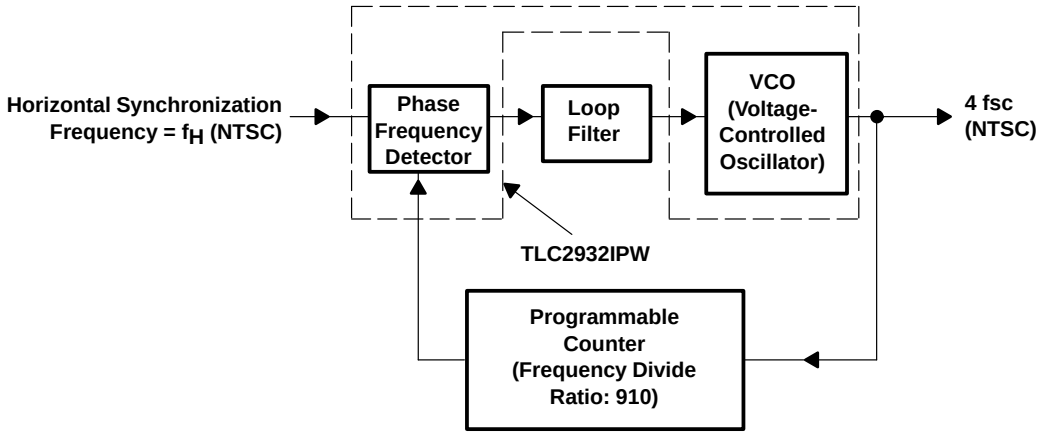
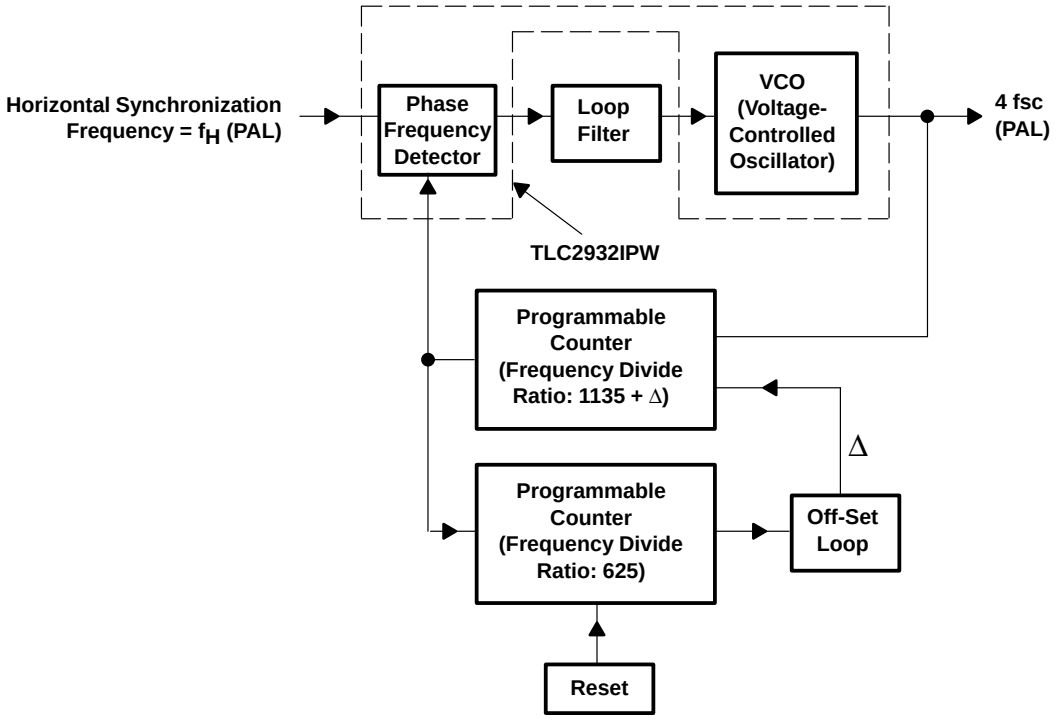


Figure 45. Generating a 4-fsc (NTSC) Signal by Multiplying the Horizontal Synchronization Frequency

5.1.2 Generating a 4-fsc PAL Signal from a PAL Signal

A phase alteration line (PAL) signal horizontal synchronization frequency (f_H) is multiplied by 1135 + Δ† to generate a 4 fsc PAL signal. Figure 46 shows a block diagram of the PLL.



† Δ (Delta) has a value of 0 or 1 in the PAL system.

Figure 46. Generating a 4-fsc (PAL) Signal by Multiplying the Horizontal Synchronization Frequency

Since 4 times the color subcarrier frequency (fsc) is not an integer multiple of the horizontal sweep frequency (fH), there must be an adjustment made in generating 4-fsc such that the average value of 4-fsc is the PAL subcarrier frequency. This averaging is accomplished by the offset loop. The value of the frequency divider is then incremented 4 times during the scan to maintain the average 4-fsc. This is illustrated in the following table.

Table 15. Offset Values for Averaging PAL 4-fsc

1135 PROGRAMMABLE DIVIDER	OFFSET 625 COUNTER	
1135 + (Delta = 0)	1 – 156	
1135 + (Delta = 1)	157	(+ 157)
1135 + (Delta = 0)	158 – 312	
1135 + (Delta = 1)	313	(+ 156)
1135 + (Delta = 0)	314 – 468	
1135 + (Delta = 1)	469	(+ 156)
1135 + (Delta = 0)	470 – 624	
1135 + (Delta = 1)	625	(+ 156)

5.1.3 Generating a 13.5-MHz Output from a NTSC or PAL Signal

Figure 47 shows the derivative of a 4-fsc signal from a PAL or NTSC horizontal synchronization frequency.

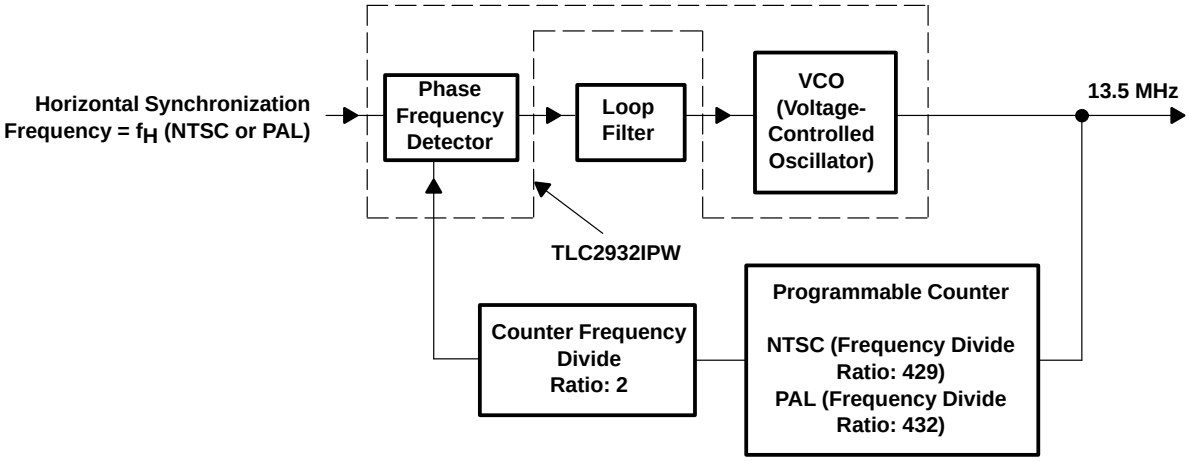


Figure 47. Multiplying the Horizontal Synchronization Frequency of a NTSC Signal or PAL Signal to Generate a 13.5 MHz Output

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